規格書
DataSheet

CUSTOMER :

Company Name

Allied Vision

Model NO :

FWB-PCIE1X11

DESCRIPTION :

Three ports FireWire 800(IEEE-1394b) to PCI Express Host Adapter

Revision :

1.1.2

CUSTOMER APPROVED	APPROVAL	ENGINEER	ISSUE BY

IOI Technology Corporation

映奧股份有限公司

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TEL : 02-89191358 FAX : 02-89191359

Contents

Overview

Highlight:

- Host Bus: 1-lane 2.5 Gb/s PCI Express
- Complies with 1394 OHCI draft 1.2
- Three external 1394 ports
- Supports Bilingual Plug port with Jackscrew Type 1394b Cable

Introduction:

FWB-PCIE1X11 is designed with Texas Instruments XIO2213B controller.
The Texas Instruments XIO2213B is a PCI Express to PCI translation bridge where the PCI bus interface is internally connected to a 1394b open host controller link-layer controller with a three-port 1394b PHY. The PCI-Express to PCI translation bridge is fully compatible with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Standard 1394b and the latest 1394 Open Host Controller Interface (OHCI) Specification.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCI Express bus and the 1394 bus at 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s.

FWB-PCIE1X11 provides full PCI Express and 1394b functionality and performance.

Specification:

PCI Express:	◆ Full x1 PCI Express Throughput ◆ Fully Compliant with PCI Express Base Specification, Revision 1.1 ◆ Utilizes 100-MHz Differential PCI Express Common Reference Clock
OHCI (Open Host Controller Interface):	◆ Fully supports provisions of IEEE P1394b-2002 ◆ Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000 ◆ Fully Compliant with 1394 Open Host Controller Interface Specification, Revision 1.1 and Revision 1.2 draft ◆ Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, 400M Bits/s, and 800M Bits/s ◆ Cable Ports Monitor Line Conditions for Active Connection To Remote Node ◆ Cable Power Presence Monitoring ◆ EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric ◆ Active State Link Power Management Saves Power When Packet Activity on the PCI Express™ Link is Idle, Using Both L0s and L1 States ◆ Support for D1, D2, D3hot
Number of Ports:	**FWB-PCIE1X11A:** Two Bilingual IEEE Std 1394b-2002 Cable Ports One FireWire IEEE Std 1394a-2000 Cable Port **FWB-PCIE1X11B:** Three Bilingual IEEE Std 1394b-2002 Cable Ports
Bus Power Connector:	Big IDE 4-pin DC Power Connector

Operating System Requirements:

The 1394b function (host driver) is supported (built in) by the following OS:
- Windows 2000 SP4 or later
- Windows XP SP2 or later
- Windows Vista SP1 or later
- Windows 8 and 8.1
- Mac OS 10.4 or later
- Linux kernel 2.6.23 or later.

RoHS:

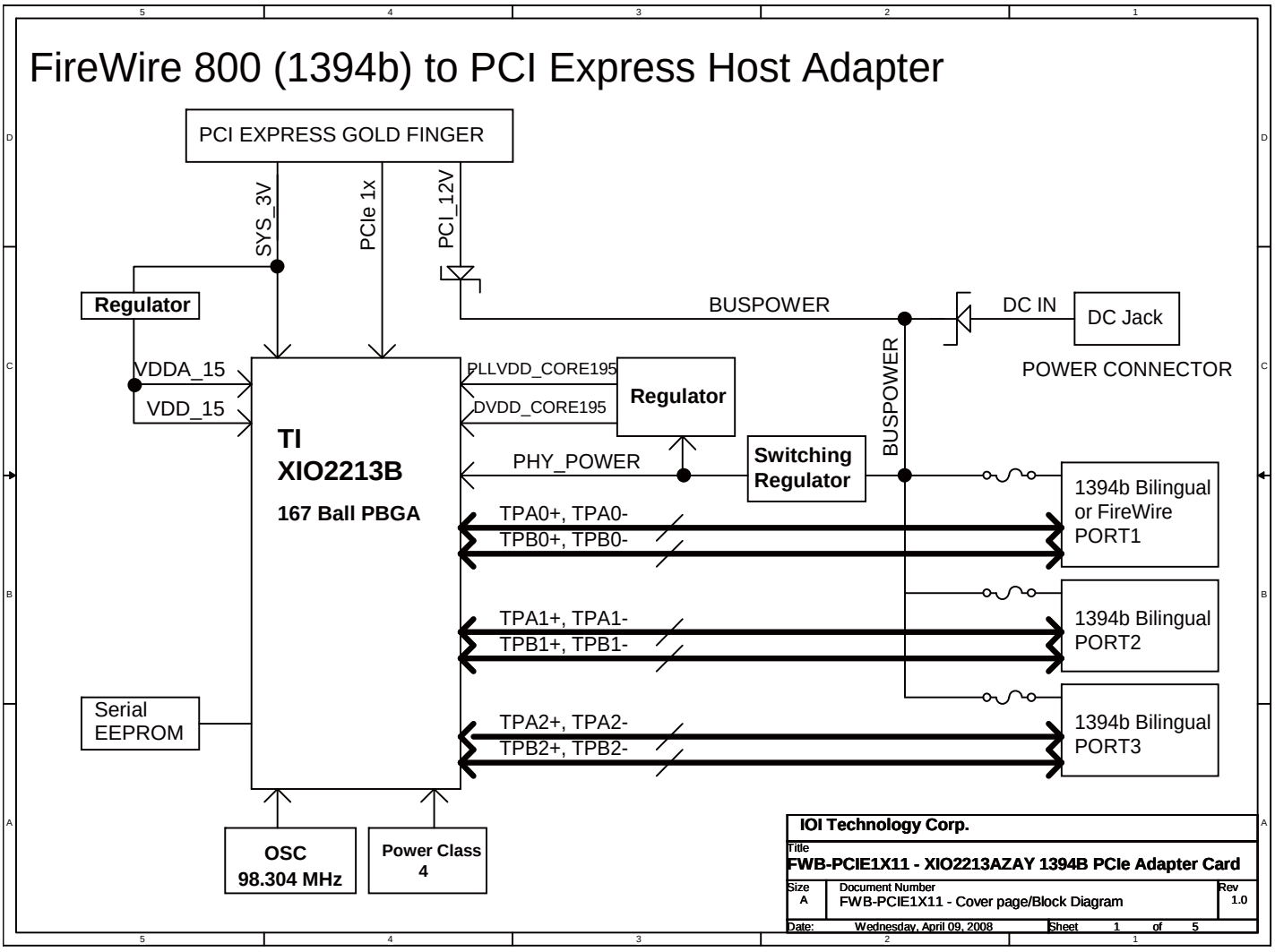
This Host Adapter is satisfied with RoHS regulations. Material of solder is satisfied with following definition.

	Material of solder
Solder Paste	SN-3.0AG-0.5CU
Flow and hand soldering	SN-0.7CU+NI

Environmental Condition:

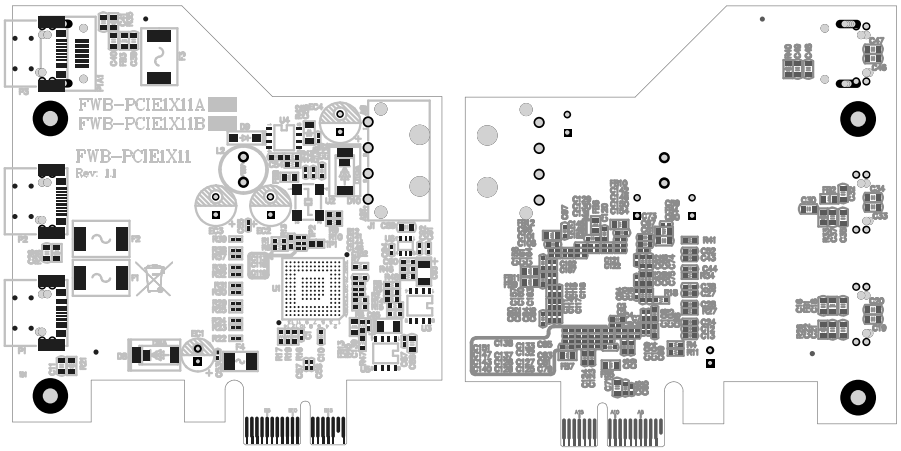
Operating free-air temperature: 0 ~ 65 degree C
Storage temperature range: -20 ~ 100 degree C
Humidity Operating : 0 ~ 80% RH, Non-condensing

Block Diagram :



Silk Screen and Pictures

Silk Screen of FWB-PCIE1x11 P.C.B. :



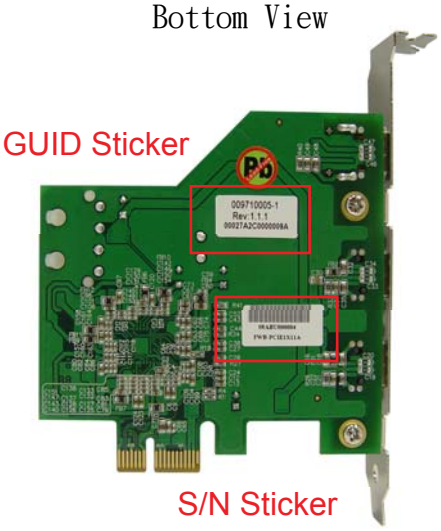
Picture of FWB-PCIE1x11 :

FWB-PCIE1X11A

Top View

Front View

Bottom View



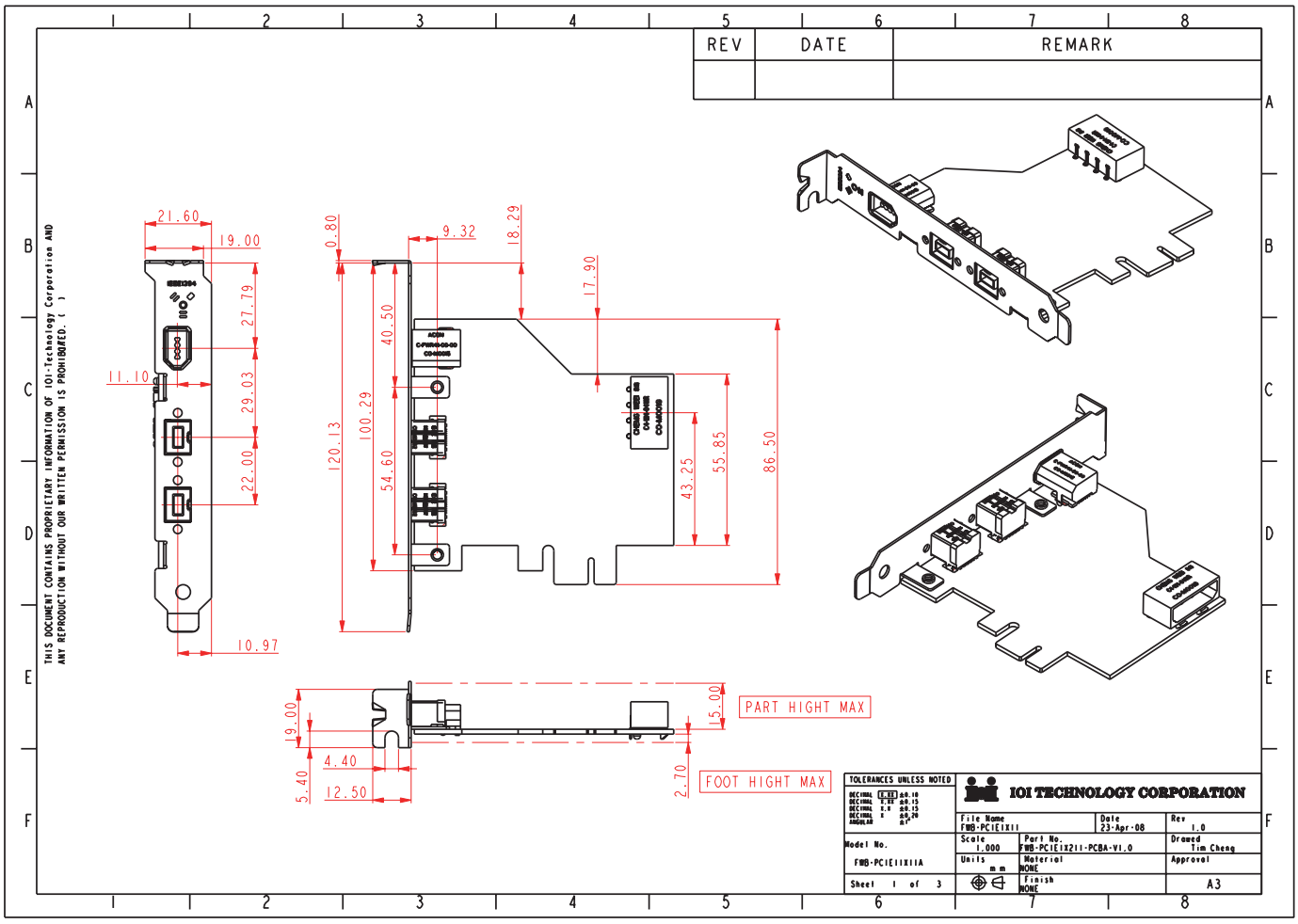
FWB-PCIE1X11B

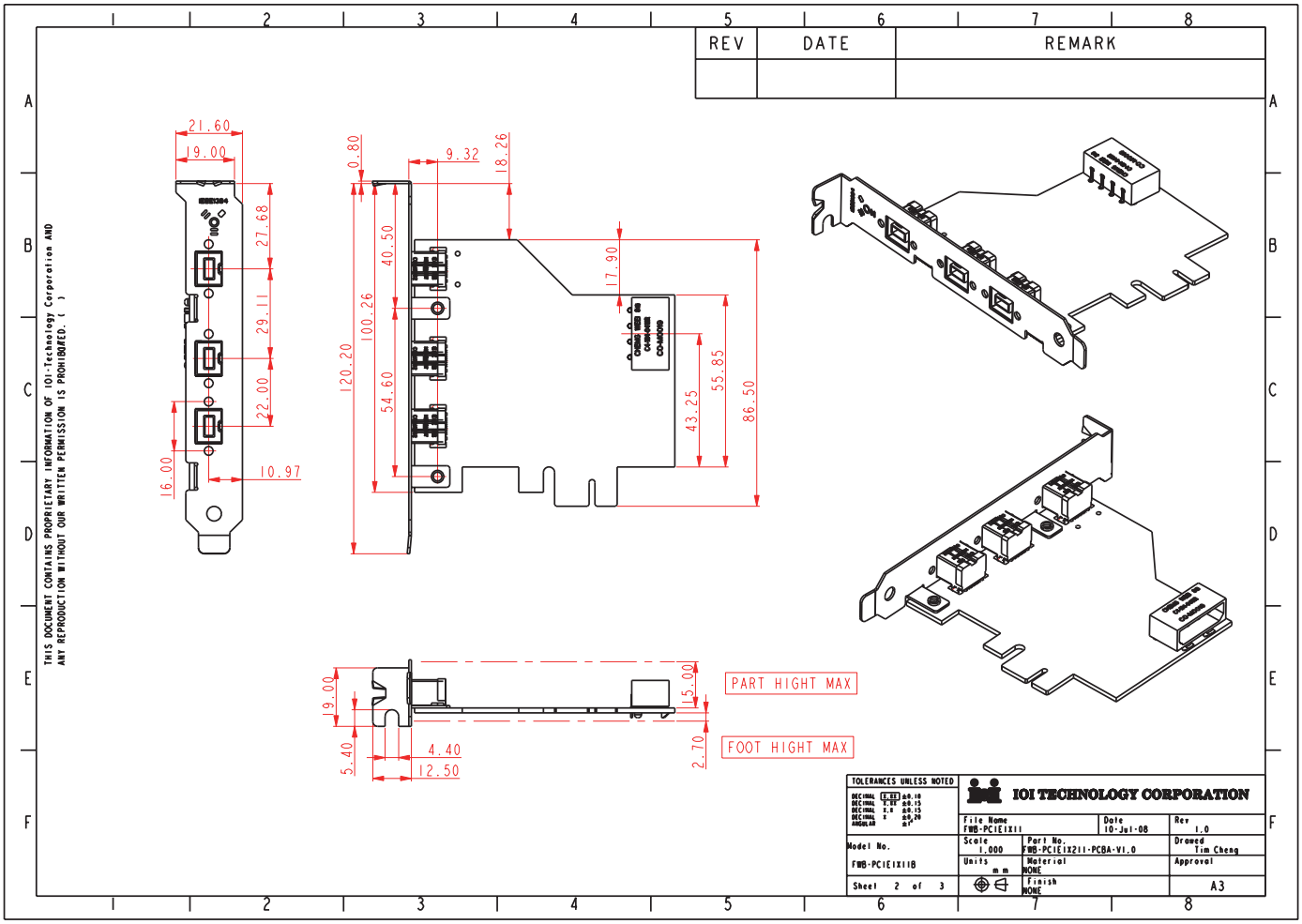
Top View

Front View

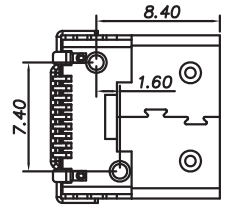
Bottom View

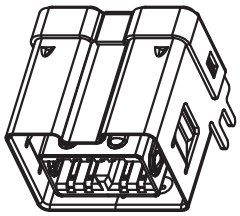
Mechanical Dimension

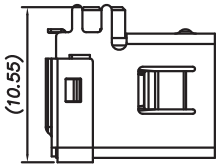


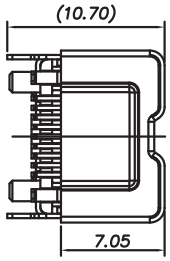


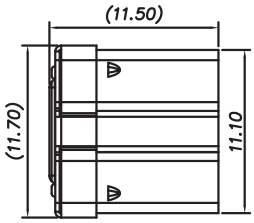
REV	DATE	REMARK

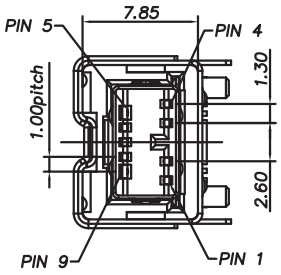








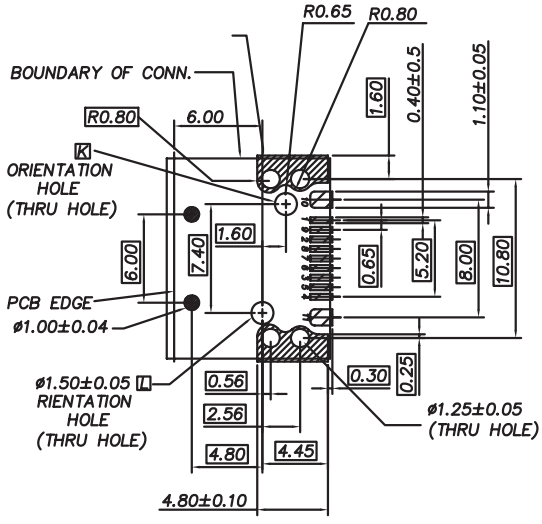




NOTES:
1) *MATERIAL:*
HOUSING: Thermoplastic, UL94V-0
CONTACT: Copper Alloy
SHELL: BRASS
2) *PLATING:*
Please refer to order information

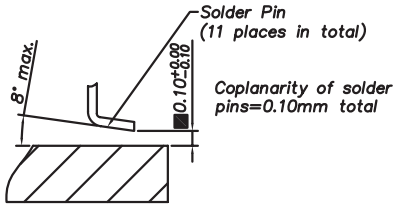
TOLERANCES UNLESS NOTED	IOI TECHNOLOGY CORPORATION		
DECIMAL X.XX ±0.10 DECIMAL X.XX ±0.15 DECIMAL X.X ±0.15 DECIMAL X ±0.20 ANGULAR ±1°	File Name CO-M0103	Date 2009/06/26	Rev 1.0
Model No. CO-M0103	Scale NONE	Part No. CO-M0103	Drawed
	Units m m	Material NONE	Approval
Sheet 1 of 2		Finish NONE	A4

REV	DATE	REMARK



PCB LAYER OUT
SCALE 5:1

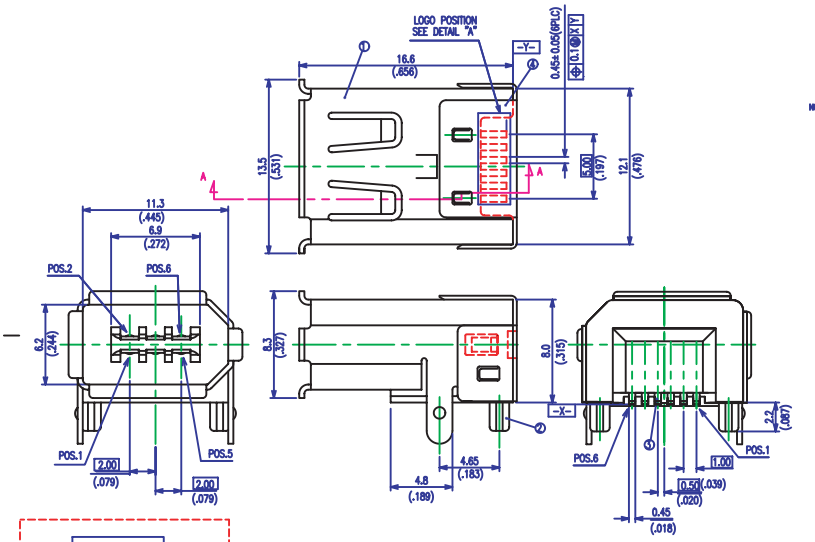
Notes:
1. *Electrical Specifications:*
Voltage: 30V
Current: 1.5 AMPS
Contact Resistance: 50mΩ max.
Shell Resistance: 50mΩ
Insulation Resistance: 100 MΩ min.
Dielectric Withstand: 100Vdc
2. *Temperature Range:*
Operating: −40℃ ~ +85℃
Storage: −40℃ ~ +105℃
3. *The Clearance Between the contact and PCB no more than 0.10mm*



View of Coplanarity

TOLERANCES UNLESS NOTED	IOI TECHNOLOGY CORPORATION		
DECIMAL X.XX ±0.10 DECIMAL X.XX ±0.15 DECIMAL X.X ±0.15 DECIMAL X ±0.20 ANGULAR ±1°	File Name CO-M0103	Date 2009/06/26	Rev 1.0
Model No. CO-M0103	Scale NONE	Part No. CO-M0103	Drawed
	Units m m	Material NONE	Approval
Sheet 2 of 2		Finish NONE	A4

REV	DATE	REMARK



NOTES: UNLESS OTHERWISE SPECIFIED:

1.0 CONNECTOR ELECTRICAL CHARACTERISTICS:
1.1 WITHSTANDING VOLTAGE: DC 500±50 V
1.2 INSULATION RESISTANCE: 100 MEGOHMS Min.
1.3 CONTACT RESISTANCE: 30 MILLIOHMS Max.
2.0 MATERIALS:
2.1 HOUSING: HIGH TEMPERATURE THERMOPLASTICS, UL94V-0.
2.2 SHELL: COPPER ALLOY
2.3 CONTACTS: COPPER ALLOY
2.4 BACK SHELL: STEEL
3.0 FINISH:
⚠ 3.1 SHELL: TIN-LEAD OR BRIGHT TIN-LEAD PLATING
⚠ OR BRIGHT TIN PLATING AND NI
⚠ 3.2 CONTACTS: PLATED GOLD IN MATING AREA; Sn-Cu ON TAILS.
4.0 OTHERS:
4.1 ALL DIMENSIONS ARE IN MILLIMETERS WITH INCH EQUIVALENTS SHOWN IN BRACKETS.
4.2 DIMENSIONING PER ANSI Y14.5M-1982.
⚠ 4.3 THE DRAWING ARE REDREW.

P/N: FWR41-6N5100

ACON

P/N: FWR41-6N5400

DETAIL "A"

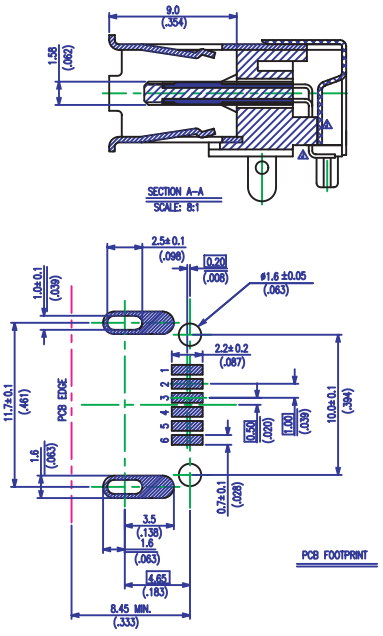
TOLERANCES UNLESS NOTED

DECIMAL	XXX	±0.10
DECIMAL	XXX	±0.15
DECIMAL	X.X	±0.15
DECIMAL	X	±0.20
ANGULAR		±1°

IOI TECHNOLOGY CORPORATION

File Name: CO-M0015		Date	Rev: 1.0
Model No.: CO-M0015	Scale: NONE	Part No.: CO-M0015	Drawed: V-0562
	Units: m m	Material: NONE	Approval
Sheet 1 of 2		Finish: NONE	A4

REV	DATE	REMARK



PRODUCT NUMBERING CODE:

FWR41 – 6 X X X 0 X
1 2 3 4 5 6

1. CONNECTOR STYLE:
FWR41: IEEE 1394 (FIREWIRE) CONNECTOR, RIGHT ANGLE, RECEPTACLE, R/M (BOARD-MOUNT),FLAT,SMT TYPE, WITH BACKSHELL, h=4.50mm
(h=CENER OF MATING FACE TO PCB)

2. NO. OF CONTACTS:
6: 6 POSITIONS.

3. COLOR OF HOUSING.
N: NATURAL COLOR.
K: BLACK COLOR.
⚠ G: PANTONE 424C

4. PLATING THICKNESS IN CONTACT MATING AREA:
⚠ 5: 30u" GOLD IN MATING AREA; Sn-Cu ON TAILS.
⚠ 2 : 5u" GOLD PLATING
⚠ 8 : 30u" Au CONTACT AREA MATT Sn TERMINATION AREA

5. PLATING OF SHELL AND MARK CHANGES: SEE TABLE A

⚠ 6. PACKAGING OF PRODUCTS
0 : TRAY
1 : TAPE & REEL

TABLE A:

	CODE	DESCRIPTION
	1	TIN-LEAD PLATING, W/O LOGO
	3	SEE DRAWING NO. C-FWR41-01-00
	4	TIN-LEAD PLATING, ACON LOGO
	5	BRIGHT TIN-LEAD PLATING, W/O LOGO
⚠	C	BRIGHT TIN PLATING, W/O LOGO
⚠	G	BRIGHT TIN PLATING, WITH ACON LOGO
⚠	J	NI PLATING, W/O LOGO
⚠	T	NI PLATING, WITH ACON LOGO
⚠	H	SEE DRAWING NO. C-FWR41-02-00

TOLERANCES UNLESS NOTED

DECIMAL	XXX	±0.10
DECIMAL	XXX	±0.15
DECIMAL	X.X	±0.15
DECIMAL	X	±0.20
ANGULAR		±1°

IOI TECHNOLOGY CORPORATION

File Name: CO-M0015		Date	Rev: 1.0
Model No.: CO-M0015	Scale: NONE	Part No.: CO-M0015	Drawed: V-0562
	Units: m m	Material: NONE	Approval
Sheet 2 of 2		Finish: NONE	A4

REV	DATE	REMARK

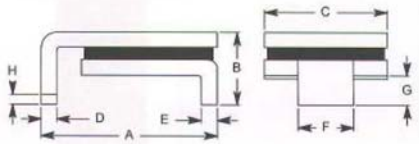
Maximum Electrical Ratings

Operating Voltage / Interrupt Current

33V / 40A
12V / 60A
5V / 125A

Marking:

153F
- Manufacturer's Mark
- Part Identification



Notes:
1. All metal surfaces are tin plated.
2. Devices cannot be wave soldered.
3. Drawing not to scale.

TABLE I. DIMENSIONS:

	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX	D MIN	D MAX	E MIN	E MAX	F MIN	F MAX	G MIN	G MAX	H MIN
mm	8.00	9.40	--	3.00	6.0	6.71	0.56	0.71	0.56	0.71	3.68	3.94	0.66	1.37	0.43
in*	(0.315)	(0.370)	--	(0.118)	(0.236)	(0.264)	(0.022)	(0.028)	(0.022)	(0.028)	(0.145)	(0.155)	(0.026)	(0.054)	(0.017)

*Rounded off approximation

TABLE II. PERFORMANCE RATINGS:

CURRENT RATINGS**						TIME TO TRIP**	RESISTANCE VALUES		TRIPPED-STATE POWER DISSIPATION**
AMPS AT 0°C		AMPS AT 20°C		AMPS AT 60°C		SECONDS AT 20°C, 8.0A	OHMS AT 20°C		WATTS AT 20°C
HOLD	TRIP	HOLD	TRIP	HOLD	TRIP	MAX	MIN	MAX*	MAX
1.80	3.60	1.50	3.00	0.99	1.98	5	0.080	0.230	1.9

* Maximum resistance is measured both 1 hour post reflow and 1 hour post trip.
** Values specified were determined using PCB's with 0.070 X1.5 ounce copper traces.

Reference Documents: PS300, E.N. SMD 1.0x
Precedence: This specification takes precedence over documents referenced herein.
Effectivity: Reference documents shall be the issue in effect on the date of invitation for bid.
CAUTION: Operation beyond the rated voltage or current may result in rupture, electrical arcing or flame.

TOLERANCES UNLESS NOTED

DECIMAL	XXX	±0.10
DECIMAL	XXX	±0.15
DECIMAL	X.X	±0.15
DECIMAL	X	±0.20
ANGULAR		±1°

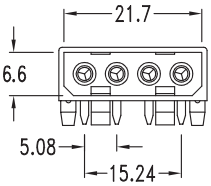
IOI TECHNOLOGY CORPORATION

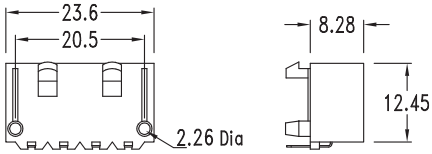
File Name: FU-S0005		Date	Rev: 1.0
Model No.: FU-S0005	Scale: NONE	Part No.: FU-S0005	Drawed: V-0562
	Units: m m	Material: NONE	Approval
Sheet 1 of 2		Finish: NONE	A4

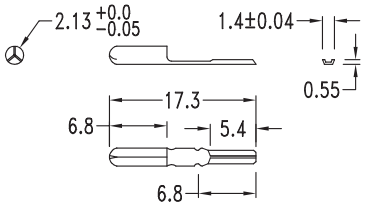
REV	DATE	REMARK

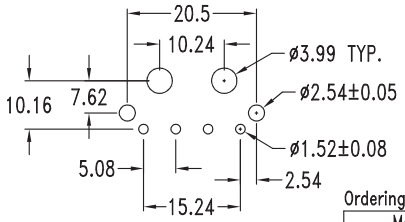
Features/Specifications:

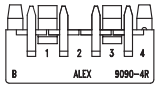
- UL 94V-2 nylon 66, Natural color
- Pins: Phosphor bronze Thickness 0.25mm
- Plating tin
- Two P.C tail lengths
- Voltage Rating: 250V AC (R.M.S)
- Current Rating: 6.5 amperes
- Dielectric Withstanding Voltage: 1500 VAC for 60 sec.
- Insulation Resistance: 500 megohms milliohms
- Contact Resistance: 10 milliohms maximun
- Ambient Temperature Range: -40°C to 105°C











Ordering Information

Model No.	P.C Tail Lengtb
CO-M0019	3.6±0.5mm

TOLERANCES UNLESS NOTED

DECIMAL XXX ±0.10
DECIMAL XXX ±0.15
DECIMAL X.X ±0.15
DECIMAL X ±0.20
ANGULAR ±1°

IOI TECHNOLOGY CORPORATION

File Name: CO-M0019		Date	Rev: 1.0
Model No.: CO-M0019	Scale: NONE	Part No.: CO-M0019	Drawed: Y-0562
	Units: m m	Material: NONE	Approval
Sheet 1 of 2		Finish: NONE	A4

1 Introduction

1.1 XIO2213B Features

- **Full ×1 PCI Express™ (PCIe) Throughput**
- **Fully Compliant With PCI Express Base Specification, Revision 1.1**
- **Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock**
- **Fully Supports Provisions of IEEE Std P1394b-2002**
- **Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000**
- **Fully Compliant With 1394 Open Host Controller Interface (OHCI) Specification, Revision 1.1 and Revision 1.2 Draft**
- **Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bit/s, 200M Bit/s, 400M Bit/s, and 800M Bit/s**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Cable Power Presence Monitoring**
- **EEPROM Configuration Support to Load Global Unique ID for 1394 Fabric**
- **Support for D1, D2, $D3_{hot}$**
- **Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link Is Idle, Using Both L0s and L1 States**
- **Eight 3.3-V Multifunction General-Purpose I/O (GPIO) Terminals**

2 Overview

The Texas Instruments XIO2213B is a single-function PCI Express™ (PCIe) to PCI local bus translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b physical layer (PHY). When the XIO2213B is properly configured, this solution provides full PCIe and 1394b functionality and performance.

2.1 Description

The TI XIO2213B is a PCIe to PCI translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b PHY. The PCIe to PCI translation bridge is fully compatible with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Std 1394b and the latest 1394 Open Host Controller Interface (OHCI) Specification.

The XIO2213B simultaneously supports up to four posted write transactions, four nonposted transactions, and four completion transactions pending in each direction at any time. Each posted write data queue and completion data queue can store up to 8K bytes of data. The nonposted data queues can store up to 128 bytes of data.

The PCIe interface supports a ×1 link operating at full 250 Mbit/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the PCI Express Base Specification, Revision 1.1. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency. If parity errors are detected, packet poisoning is supported for both upstream and downstream operations.

PCIe power management (PM) features include active-state link PM, PME mechanisms, and all conventional PCI D states. If the active-state link PM is enabled, the link automatically saves power when idle using the L0s and L1 states. PM active-state NAK, PM PME, and PME-to-ACK messages are supported. The bridge is compliant with the latest PCI Bus Power Management Specification and provides several low-power modes, which enable the host power system to further reduce power consumption

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCIe configuration space, allow for further system control and customization.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCIe bus and the 1394 bus at 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s. The device provides three 1394 ports that have separate cable bias (TPBIAS).

As required by the 1394 Open Host Controller Interface (OHCI) Specification, internal control registers are memory mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCIe, and it provides plug-and-play (PnP) compatibility.

The PHY provides the digital and analog transceiver functions needed to implement a 3-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An optional external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.

The XIO2213B requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL. Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbit/s (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

To ensure that the XIO2213B conforms to IEEE Std 1394b-2002, the BMODE terminal must be asserted. The BMODE terminal does not select the cable-interface mode of operation. BMODE selects the internal PHY-section/LLC-section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the XIO2213B, this bit can only be set by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.