Pike

Technical Manual

V5.2.4

2018-Dec-14

Allied Vision Technologies GmbH
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Allied Vision

Contents

Contacting Allied Vision

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www.alliedvision.com/en/contact

Find an Allied Vision office or distributor:

www.alliedvision.com/en/about-us/where-we-are.html

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info@alliedvision.com (for commercial and general inquiries)
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Introduction

This Pike Technical Manual describes in depth the technical specifications, dimensions, all camera features (IIDC standard and Allied Vision smart features) and their registers, trigger features, all video and color formats, bandwidth, and frame rate calculation.

For information on hardware installation, safety warnings, and pin assignments on I/O connectors and 1394b connectors read the 1394 Installation Manual.

Note

Please read through this manual carefully.

We assume that you have read already the 1394 Installation Manual (see: http://www.alliedvision.com/en/support/technical-documentation) and that you have installed the hardware and software on your PC or laptop (FireWire card, cables).

Document history

Version	Date	Remarks
V2.0.0	2006-Jul-07	New Manual- RELEASE status
PRE_V3.0.0	2006-Sep-22	Minor corrections Added Pike F-145 Pike F-210 AOI frame rates corrected: Chapter Pike F-210: AOI frame rates (no sub-sampling) on page 233 New advanced registers: Chapter Advanced features on page 287
V3.0.1	2006-Sep-29	Minor corrections
V3.1.0	2007-Feb-13	Changed camera status register (Table 157: Advanced register: Camera status on page 295) Added description for the following mode *Output state follows PinState bit (Table 32: Output routing* on page 92*)* Added M39-Mount for Pike F-201 and F-421 (Chapter F-Mount on page 73)

Table 1: Document history

Version	Date	Remarks
V3.2.0	2007-Aug-22	Minor corrections Added CE in Chapter Conformity on page 33. Added Value field in Table 44: CSR: Shutter on page 113. Added Chapter Cross section: CS-Mount (Pike F-032B, F-032C) on page 70. Added detailed description of BRIGHTNESS (800h) in Table 150: Feature control register on page 282 Added detailed description of WHITE-BALANCE (80Ch) in Table 150: Feature control register on page 282 et seq. Added Appendix, Chapter on page 378. Added new frame rates in Chapter Specifications on page 45 Added new AOI frame rates and diagrams in Chapter Frame rates Format_7 on page 226 New minimum shutter speeds for each of the Pike cameras in Chapter Specifications on page 45 and the following Added new features of Pike update round: • SIS: see Chapter Secure image signature (SIS): definition and scenarios on page 198 • Sequence mode: see Chapter Sequence mode on page 190 • Smear reduction see Chapter Smear reduction (not Pike F-1100, F-1600) on page 200 • 4 x / 8 x binning and sub-sampling modes see Chapter Binning (monochrome models only) on page 139 see Chapter Sub-sampling (monochrome and color models) on page 143 see Chapter Binning and sub-sampling access on page 150 • Quick mode for format changes see Chapter Quick parameter change timing modes on page 153 • Speed increase mode (Packed 12-bit Mode) Chapter Packed 12-Bit Mode on page 158 • CS-Mount (only for Pike F-032) Chapter Pike F-032B, F-032C (fiber) on page 45 and Chapter Cross section: CS-Mount (Pike F-032B, F-032C) on page 70

Table 1: Document history

Version	Date	Remarks
V4.0.0	2008-Jan-15	Added 15fps versions of Pike F-145 at Table 155: Camera type ID list on page 292 Added VERSION_INFO1_EX, VERSION_INFO3_EX and description at Table 154: Advanced register: Extended version information on page 291 Revised Chapter Secure image signature (SIS) on page 323 Added detailed description to register 0xF10000570 PARAMUPD_TIMING (how to switch on Quick Format Change Mode) see Chapter Quick parameter change timing modes on page 317 Added Chapter Pike F-505B, F-505C (fiber) on page 55. Added Chapter Pike F-505B, F-505C on page 213. Revised description of C-Mount adjustment in Chapter C-Mount adjustment on page 72. Moved Allied Vision Glossary from Appendix of Pike Technical Manual to Allied Vision Website. Revised Pike F-505B/C data. Corrected binning (only b/w cameras) and added Format_IDs in Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152.

Table 1: Document history

Version	Date	Remarks
V4.1.0	2008-Aug-20	Added Pike F-505 to Chapter Index on page Index Revised formulas by adding some units in Chapter How does bandwidth affect the frame rate? on page 254 Corrected Table 175: Advanced register: Channel balance on page 313 Added Max IsoSize Bit [1] to register 0xF1000048 ADV_INQ_3 in Table 156: Advanced register: Advanced feature inquiry on page 293f. Added Chapter Maximum ISO packet size on page 315 (useful for Pike F-505 for higher frame rates) Corrected Figure 71: Former standard timing on page 153 Added photos of 1394b locking connectors and 1394a Molex clamp locking (aka Interlock) connectors in Chapter 1394a and 1394b cameras and compatibility on page 39. Added recommendation to use PCI-X (64 bit) or PCI Express adapter in Chapter Maximum ISO packet size on page 315. Corrected frame rate formula in Chapter High SNR mode (High Signal Noise Ratio) on page 158. Corrected binning order in Chapter 2 × full binning, 4 × full binning, 8 × full binning on page 142. Added block diagram of modern PC (X38 chipset by INTEL) in Figure 5: Block diagram of modern PC (X38 chipset by INTEL) on page 39 Revised FireWire hot-plug precautions and added screw-lock precautions in Chapter FireWire hot-plug and screw-lock precautions on page 44 Added images of FireWire locking cables in Figure 4: 1394a and 1394b cameras and compatibility on page 39 Added list of available FireWire screw lock cables in Table 4: 1394 locking cables on page 35 Corrected CAD drawing in Figure 26: Pike W90 S90 (2 x 1394b copper) on page 73 Changed provisions directive to 2004/108/EG in Chapter Conformity on page 33 Corrected diag. (16.3 mm) of KAI2093 in Table 11: Pike F-210B (fiber) model specifications on page 51

Table 1: Document history

Version	Date	Remarks
V4.1.0 [continued]	2008-Aug-20 [continued]	Restructuring of Pike Technical Manual: Added Chapter Contacting Allied Vision on page 12 Added Chapter Manual overview on page 25 Restructured Chapter *Pike types and highlights* to Chapter Pike cameras on page 30. Infos from *Pike camera types* table moved to Chapter Specifications on page 45 *Safety instructions* moved to *Hardware Installation Guide*, Chapter *Safety instructions* and *Camera cleaning instructions* Environmental conditions moved to *Pike Instruction Leaflet* Infos on CS-/C-Mounting moved to Hardware Installation Guide, Chapter *Changing filters safety instructions* Infos on *System components* and *Environmental conditions* moved to *Pike Instruction Leaflet* Infos on *IR cut filter* and *Lenses* moved to Chapter Filter and lenses on page 77 Moved binning explanation from Chapter Specifications on page 45 to Chapter Video formats, modes and bandwidth on page 201 Binning / sub-sampling modes and color modes are only listed in Chapter Video formats, modes and bandwidth on page 201 Moved detailed description of the camera interfaces (FireWire, I/O connector), ordering numbers and operating instructions to the *Hardware Installation Guide*. Revised Chapter Description of the data path on page 132 Revised Chapter Controlling image capture on page 174; User profiles are only described in Chapter User profiles on page 330 Revised Chapter Video formats, modes and bandwidth on page 201 Revised Chapter How does bandwidth affect the frame rate? on page 254 [to be continued]

Table 1: Document history

Version	Date	Remarks
V4.1.0 [continued]	2008-Aug-20 [continued]	[continued: Restructuring of Pike Technical Manual:] Revised Chapter Configuration of the camera on page 258 Revised Chapter Firmware update on page 337 Added Chapter on page 378 Revised Chapter Index Corrected for all Pike cameras: 16 user-defined LUTs in Chapter Specifications on page 45ff. Added cross-reference from upload LUT to GPDATA_BUFFER in Chapter Loading an LUT into the camera on page 131. Added cross-reference from upload/download shading image to GPDATA_BUFFER in: Chapter Loading a shading image out of the camera on page 127 Chapter Loading a shading image into the camera on page 128 Added Pike F-505 as it uses different BAYER pattern (first pixel of the sensor is RED) in Chapter Color interpolation (Bayer demosaicing) on page 163 Added detailed level values of I/Os in Chapter Camera I/O connections on page 82. Added RoHS in Chapter Conformity on page 33 Added little endian vs. big endian byte order in Chapter GPDATA_BUFFER on page 335 Pike update firmware round: Gain references: see Chapter User adjustable gain references on page 336 Low-noise binning mode for 2 x horizontal binning: see Chapter Low-noise binning mode (only 2 × H-binning) on page 319 New photo of LED positions in Figure 26: Position of status LEDs on page 84
V4.2.0	2008-Sep-01	New default gain references for Pike F-505B/C in Table 202: Default gain references of Pike models on page 336

Table 1: Document history

Version	Date	Remarks
V4.3.0	2009-Apr-23	Pike F-100B: new Quantum efficiency diagram in Figure 6: Pike F-100B, F-100C (ON Semiconductor KAI-1020) absolute QE on page 62 All advanced registers in 8-digit format beginning with 0xF1... in Chapter Advanced features on page 287ff. and in Table 184: Advanced register: Parameter-List Update: parameter list on page 321 Corrected Pike cameras with small (VGA size) and large filter in Chapter Cross section: C-Mount (VGA size filter) on page 70 and Chapter Cross section: C-Mount (large filter) on page 71 SEQUENCE_RESET register moved to SEQUENCE_STEP register (0xF1000228) in SEQUENCE_STEP on page 192 and in SEQUENCE_STEP on page 287. Revised Chapter White balance on page 107ff. New sensor for Pike F-421B/C in Table 3: Pike models, resolution, and frame rates on page 31 and in Table 12: Pike F-421B, F-421C (fiber) model specifications on page 53. Calculated effective chip size for all sensors (with resolution of Format_7 Mode_0) in Chapter Specifications on page 45ff. Pike F-210B/C shows no speed increase using sub-sampling: see Chapter Pike F-210: AOI frame rates (sub-sampling) on page 234

Table 1: Document history

<table>
<tr><th>Version</th><th>Date</th><th>Remarks</th></tr>
<tr><td>V4.4.0</td><td>2009-Sep-28</td><td>Added notice to description of non-volatile storage of shading image in Note on page 125.

Corrected drawing in Figure 116: Delayed integration timing on page 307

Corrected Format_7 Mode_5 (640 x 240) in Table 85: Video Format_7 default modes Pike F-032B, Pike F-032C on page 203.

Added Raw12 to Pike F-032C and corrected some frame rates in Table 85: Video Format_7 default modes Pike F-032B, Pike F-032C on page 203f.

New dual-tap offset adjustment for Pike F-032/210/421/505:
• See 0xF1000430 on page 289
• See Table 176: Advanced register: Dual-tap offset adjustment on page 313
• See Chapter Dual-tap offset adjustment with SmartView (1.10 or greater) on page 105
• Revised Chapter Conformity on page 33.
New Pike front flange:
• Title page: new photo and Figure 18: Back focus adjustment on page 72: new Pike drawing
• New CAD drawings:
– Chapter Camera dimensions on page 66ff.
– Figure 18: Back focus adjustment on page 72 (adjusting C-Mount via both screws on top (middle) and right sight of the housing
Added PWM feature:
• Added PWM feature in IO_OUTP_CTRL 1-4 on page 91ff.
• Added PWMCapable in Register 0xF1000320 in Table 31: Advanced register: Output control on page 91
• Added ID 0x09 in Table 32: Output routing on page 92
• Added Chapter Pulse-width modulation on page 94ff.
• Added Table 33: PWM configuration registers on page 94
• Added PWM in Table 156: Advanced register: Advanced feature inquiry on page 293f.
• Added PWM in Table 153: Advanced registers summary on page 287ff.</td></tr>
</table>

Table 1: Document history

Version	Date	Remarks
V4.4.0 [continued]	2009-Sep-28 [continued]	• All Pike models: added input debounce feature: – Advanced register summary `0xF1000840` on page 290 – Advanced register summary `0xF1000850` on page 290 – Advanced register summary `0xF1000860` on page 290 – Advanced register summary `0xF1000870` on page 290 – Chapter Debounce on page 181f. – Chapter Debounce time on page 182 – Table 72: Advanced register: **Debounce time for input ports** on page 182 • All Pike models: added Frame time control feature: – Table 153: Advanced registers summary on page 287ff. – Chapter Frame time control on page 334
V5.0.0	2010-May-07	• New Pike F-1100 and Pike F-1600 models: • Figure 11: Pike F-1100B, F-1100C (ON Semiconductor KAI-11002) absolute QE on page 64 • Figure 18: Spectral sensitivity of Pike F-1100C on page 70 • Figure 12: Pike F-1600B, F-1600C (ON Semiconductor KAI-16000) absolute QE on page 65 • Figure 20: Spectral sensitivity of Pike F-1600C on page 71 • Chapter Pike F-1100B, F-1100C (fiber) on page 57 • Chapter Pike F-1600B, F-1600C (fiber) on page 59 • Chapter Pike F-1600B, F-1600C (fiber) on page 59 • Chapter Dual-tap offset adjustment with SmartView (1.10 or greater) on page 129ff. and Chapter Chapter Dual-tap offset adjustment on page 313. • Chapter F-Mount adjustment for Pike F-1100 and Pike F-1600 on page 76 • Chapter F-Mount on page 73 • Chapter F-Mount adjustment for Pike F-1100 and Pike F-1600 on page 76 • Chapter F-Mount on page 73 • Chapter Pike F-Mount: standard housing (2 x 1394b copper) on page 84 • Chapter Tripod adapter dimensions on page 82 • Chapter Pike F-Mount: W270 (2 x 1394b copper) on page 87 • Chapter Cross section on page 85 • Chapter Frame time control on page 334 • Chapter Sensor digitization taps (Pike F-1100, F-1600 only) on page 321

Table 1: Document history

Version	Date	Remarks
V5.0.0 [continued]	2010-May-07 [continued]	[continued] New Pike F-1100 and Pike F-1600 models: • Chapter F-Mount on page 73ff. • Chapter M42-Mount on page 80ff. • Chapter M58-Mount on page 84ff. • Chapter Exposure time offset on page 183 • Chapter Minimum exposure time on page 183 • Figure 81: Data flow and timing after end of exposure on page 187 • Table 79: Jitter at exposure start (no binning, no sub-sampling) on page 189 • Table 202: Default gain references of Pike models on page 336 • Chapter Software feature control (disable LEDs / switch single-tap and dual-tap) on page 319 • Chapter Pike F-1100B, F-1100C on page 215 • Chapter Pike F-1600B, F-1600C on page 217 • Chapter Pike F-1100: AOI frame rates on page 238ff. • Chapter Pike F-1600: AOI frame rates on page 246ff. New Pike front flange: • Serial numbers for Pike camera models starting new front flange: Chapter Serial numbers for new front flange on page 66 • Added photo of Pike 11M/16M on title page Minor corrections and improvements: • Improved description on low noise binning: Chapter Low-noise binning mode (only 2 × H-binning) on page 319 • Corrected MaxValue from [0..31] to [6..31] in Table 169: Advanced register: Auto shutter control on page 307 • Corrected: Pike F-145C has Raw12 formats (F7M0, F7M4, F7M5, F7M6) in Table 89: Video Format_7 default modes Pike F-145B, F-145C on page 207 • Improved description of debounce feature in Chapter Debounce on page 181 New storage temperature: • 70 °C, see Chapter Specifications on page 45ff.

Table 1: Document history

Version	Date	Remarks
V5.0.0 [continued]	2010-May-07 [continued]	New links to the new Allied Vision website: • Chapter Contacting Allied Vision on page 12 New measured sensitivity curves: • Chapter Absolute QE on page 61ff. Added new CAD drawings for W90S90 and W270S90: • Chapter W90 S90 housing dimensions on page 72 • Chapter Pike W270 S90 (2 x 1394b copper) on page 77 • Chapter Pike W90 S90 (1394b: 1 x GOF, 1 x copper) on page 74 • Chapter Pike W270 S90 (1394b: 1 x GOF, 1 x copper) on page 78 Added more information on operating system support (Windows XP SP3, Vista SP2, Windows 7): • Chapter Operating system support on page 46 Changed sensitivity curves for Pike F-421B/C from Kodak KAI 4021 to Kodak KAI 4022: • Figure 9: Pike F-421B, F-421C (ON Semiconductor KAI-04022) absolute QE on page 63 • Figure 14: Spectral sensitivity of Pike F-421C on page 68
V5.0.1	2010-Jun-08	Minor corrections • Added red font to Pike F-1100C and Pike F-1600C in headline: see Chapter Pike F-1100B, F-1100C on page 215 and Chapter Pike F-1600B, F-1600C on page 217 • Added missing Pike F-100: see Chapter Dual-tap offset adjustment with SmartView (1.10 or greater) on page 105f. • Changed frame rates from Pike F-505 (maxBPP=1100) form 15 fps to 14 fps for RAW8 and AOI height of 2054 and 2048. Changed all frame rates that exceeded the theoretical frame rate of the CCD: see Table 116: Frame rates as function of AOI height [width=2452] (maxBPP=11000) on page 237 and Chapter Pike F-505B, F-505C (fiber) model specifications on page 55 • Changed all frame rates that exceeded the theoretical frame rate of the CCD: see Chapter Frame rates Format_7 on page 226ff.

Table 1: Document history

Version	Date	Remarks
V5.0.1 [continued]	2010-Jun-08 [continued]	Changed and new CAD drawings for Pike F-1100/1600: • Changed CAD drawings with corrected mount dimensions: see Figure 22: F-Mount cross section (Pike F-1100 and Pike F-1600) on page 76, Figure 48: Pike M42-Mount dimensions (optional for Pike F-1100 and Pike F-1600) on page 96 and Figure 32: M58-Mount cross section (Pike F-1100 and Pike F-1600) on page 87. • Added CAD drawings for Pike F-1100/1600 GOF versions incl. W270 models: Chapter Camera dimensions on page 66ff.
V5.0.2	2010-Aug-09	Changed sensitivity curve: • For Pike F-032B: due to new KODAK sensor data sheet for KAI-0340, the new sensitivity curve was added, see Figure 5: Pike F-032B, F-032C (ON Semiconductor KAI-0340) absolute QE on page 61. Changed trigger diagram: • Added trigger delay and connection between trigger delay and Busy signal, see Figure 30: Output impulse diagram on page 93 New file format: • Converted FrameMaker files from FM7 to FM9 Improved description of HSNR mode: • Added info that for 8-bit video modes, the internal HSNR calculations are done with 14 bit: Chapter High SNR mode (High Signal Noise Ratio) on page 158
to be continued on next page		

Table 1: Document history

Version	Date	Remarks
V5.1.0	2011-May-03	Added new features: Defect pixel correction • Chapter Defect pixel correction (Pike F-1100, F-1600 only) on page 132 • Advanced feature registers: see Chapter Defect pixel correction on page 329 • Advanced registers summary: see DEFECT_PIXEL_CORRECTION_CTRL on page 289 Pike F-505C • Added Pike F-505C in Figure 43: Mirror and Bayer order on page 121 Added new address: • Added Singapore address in Chapter Contacting Allied Vision on page 12 Revised chapters: • Revised Chapter Description of video data formats on page 97
V5.1.1	2012-Feb-27	VC50 variants have also the following conformities: • REACH • China RoHS See Chapter Conformity on page 33. Smaller corrections: • Pike F-1100/1600 don't have smear reduction: – Chapter Smear reduction (not Pike F-1100, F-1600) on page 200 – Smear reduction on page 294 – Chapter Smear reduction (not Pike F-1100, F-1600) on page 328 • Up to 16 LUTs can be stored permanently in the camera via 4 user sets: see Chapter Stored settings on page 332
V5.1.2	2012-Aug-13	• High SNR mode: Added note to set grab count and activation of HighSNR in one single write access: – see Chapter High SNR mode (High Signal Noise Ratio) on page 158 – Chapter High SNR mode (High Signal Noise Ratio) on page 315

Table 1: Document history

Version	Date	Remarks
V5.1.2 [continued]	2012-Aug-13 [continued]	Changed IR cut filter to *(type Jenofilt 217)*: see Figure 23: Approximate spectral transmission of IR cut filter (may vary slightly by filter lot) (type Jenofilt 217) on page 77 Pike trigger input voltage (GPIn1 and GPIn2) changed from 2 V to 3 V at min. input current of 5 mA, see Chapter Camera I/O connections on page 82.
V5.1.3	2012-Nov-19	Corrected register offset of LOW_NOISE_BINNING (0xF10005B0 instead of 0xF1000580), see: • Table 153: Advanced registers summary on page 287 • Table 182: Advanced register: Low-noise binning mode on page 319 • Chapter Index
V5.2.0	2015-Mar-09	Updated data: • Corrected hyperlinks to targets on the Allied Vision website • Removed outdated information in Chapter Requirements for PC and IEEE1394b on page 41 • Added hyperlink to FireWire accessories on the Allied Vision website in Chapter Requirements for PC and IEEE1394b on page 41 • Removed information on the Universal Package in Chapter Operating system support on page 44 • Reduced to the current information on the system requirements in Chapter Operating system support on page 44 • Added information that all color modes in Chapter Specifications on page 45 comply with the IIDC specifications • Updated sensor curves in Chapter Absolute QE on page 61. • Corrected information in Chapter Sensor position accuracy on page 339 • Adapted addresses in Chapter Contacting Allied Vision on page 10 • Corrected information for binning in Chapter Definition on page 139. Layout changes due to a changed Corporate identity: • Replaced the previous Allied Vision logo by the current one • Reworded all appropriate contents from AVT and Allied Vision Technologies to Allied Vision

Table 1: Document history

Version	Date	Remarks
V5.2.1	2017-Feb-10	Corrected maximum framerate for Pike F-505 Added a note about Hirose I/O connectors in Camera I/O connector pin assignment. Updated the absolute QE plots for Pike models with ON Semiconductor CCD sensors to reflect the changes in the Gen 2 CFA material change made by ON Semiconductor. Updated the absolute QE plots for Pike models with Sony Semiconductor CCD sensors and added spectral response plots. Removed the Pike F-210C. For more information, refer to the Product Change Notification on the Allied Vision website. Various minor corrections
V5.2.2	2017-Apr-07	Added a note about Hirose I/O connectors in Chapter Camera I/O connections on page 82 Updated note about accuracy of measurements for quantum efficiency.
V5.2.3	2018-Jan-05	Removed housing options with angled heads. Removed lens mount options for M39-, K-, M42-, M58-, and CS-Mount. Removed information on optional accessories. Applied minor changes.
V5.2.4	2018-Dec-14	Applied minor changes. Corrected typos.

Table 1: Document history

Manual overview

This manual overview describes each chapter of this manual shortly.

- Chapter Contacting Allied Vision on page 10 lists Allied Vision contact data for both:
  - Technical information / ordering
  - Commercial information
- Chapter Introduction on page 11 (this chapter) gives you the document history, a manual overview and conventions used in this manual (styles and symbols). Furthermore you learn how to get more information on

how to install hardware (1394 Installation Manual), available Allied Vision software (incl. documentation) and where to get it.

- Chapter Pike cameras on page 30 gives you a short introduction to the Pike cameras with their FireWire technology. Links are provided to data sheets and brochures on Allied Vision website.
- Chapter Compliance and intended use on page 32 gives you information about conformity and intended use of Allied Vision cameras.
- Chapter FireWire on page 34 describes the FireWire standard in detail, explains the compatibility between 1394a and 1394b and explains bandwidth details (incl. Pike examples).
  - Read and follow the FireWire hot-plug and screw-lock precautions in Chapter FireWire hot-plug and screw-lock precautions on page 44.
  - Read Chapter Operating system support on page 46.
- Chapter Filter and lenses on page 77 describes the IR cut filter and suitable camera lenses.
- Chapter Specifications on page 45 lists camera details and spectral sensitivity diagrams for each camera type.
- Chapter Camera dimensions on page 66 provides CAD drawings of standard housing (copper and GOF) models, tripod adapter, and a cross sections of C-Mount.
- Chapter Camera interfaces on page 81 describes in detail the inputs/outputs of the cameras (incl. Trigger features). For a general description of the interfaces (FireWire and I/O connector) see 1394 Installation Manual.
- Chapter Description of the data path on page 132 describes in detail IIDC conform as well as Allied Vision-specific camera features.
- Chapter Controlling image capture on page 174 describes trigger modes, exposure time, one-shot/multi-shot/ISO_Enable features. Additionally special Allied Vision features are described: sequence mode and secure image signature (SIS).
- Chapter Video formats, modes and bandwidth on page 201 lists all available fixed and Format_7 modes (incl. color modes, frame rates, binning/sub-sampling, AOI=area of interest).
- Chapter How does bandwidth affect the frame rate? on page 254 gives some considerations on bandwidth details.
- Chapter Configuration of the camera on page 258 lists standard and advanced register descriptions of all camera features.
- Chapter Firmware update on page 337 explains where to get information on firmware updates and explains the extended version number scheme of FPGA/µC.
- Chapter Appendix on page 377 lists the sensor position accuracy of Allied Vision cameras.
- Chapter Index on page Index gives you quick access to all relevant data in this manual.

Conventions used in this manual

To give this manual an easily understood layout and to emphasize important information, the following typographical styles and symbols are used:

Styles

Style	Function	Example
Bold	Programs, inputs or highlighting important things	bold
Courier	Code listings etc.	Input
Upper case	Register	REGISTER
Italics	Modes, fields	*Mode*
Parentheses and/or blue	Links	(Link)

Table 2: Styles

Symbols

Note

This symbol highlights important information.

Caution

This symbol highlights important instructions. You have to follow these instructions to avoid malfunctions.

www

This symbol highlights URLs for further information. The URL itself is shown in blue.

Example:

http://www.alliedvision.com

More information

For more information on hardware and software read the following:

- 1394 Installation Manual describes the hardware installation procedures for all 1394 cameras (Marlin, Guppy, Pike, Stingray). Additionally, you get safety instructions and information about camera interfaces (IEEE1394a/b copper and GOF, I/O connectors, input and output).

www

You find the 1394 Installation Manual here:

http://www.alliedvision.com/en/support/technical-documentation

www

All software packages (including documentation and release notes) provided by Allied Vision can be downloaded at:

http://www.alliedvision.com/en/support/software-downloads

Before operation

We place the highest demands for quality on our cameras.

Target group This Technical Manual is the guide to detailed technical information of the camera and is written for experts.

Getting started For a quick guide how to get started read 1394 Installation Manual first.

Note

Please read through this manual carefully before operating the camera.

For information on Allied Vision accessories and software read 1394 Installation Manual.

Caution

Before operating any Allied Vision camera read safety instructions and ESD warnings in 1394 Installation Manual.

Note

To demonstrate the properties of the camera, all examples in this manual are based on the FirePackage OHCI API software and the SmartView application.

Note

The camera also works with all IIDC (formerly DCAM) compatible IEEE 1394 programs and image processing libraries.

All naming in this document relates to FirePackage, not to GenICam.

www

For downloads see:

Software (Vimba and all other software): http://www.alliedvision.com/en/support/software-downloads

Firmware: http://www.alliedvision.com/en/support/firmware

Technical documentation (overview page): http://www.alliedvision.com/en/support/technical-documentation

Technical papers (appnotes, white papers) and knowledge base: http://www.alliedvision.com/en/support/technical-papers-knowledge-base

Pike cameras

Pike The Pike is a fast IEEE1394b camera for demanding applications. Numerous pre-processing functions produce an outstanding image quality. Pike cameras can be operated with very high frame rates and offer more real-time functions than specified in the IIDC standards.

They can even emulate traditional frame grabber functions.

IEEE1394b IEEE1394b provides a plug & play interface standard with high-speed, deterministic data transmission. The camera communication protocol is standardized and can easily be integrated into your application

GOF Pike cameras are available both with two copper ports (for daisy-chaining) and with copper/GOF (glass optical fiber) ports.

Advantages of GOF:

- 800 Mbit/s over 400 meters and more
- No additional repeaters required
- Transmission of light instead of electricity: No ground problems and no interference with electromagnetic fields.

Image applications Allied Vision can provide users with a range of products that meet almost all the requirements of a very wide range of image applications.

FireWire The industry standard IEEE1394 (FireWire or i.Link) facilitates the simplest computer compatibility and bidirectional data transfer using the plug & play process. Further development of the IEEE1394 standard has already made 800 Mbit/second possible. Investment in this standard is therefore secure for the future; each further development takes into account compatibility with the preceding standard, and vice versa, meaning that IEEE1394b is reverse-compatible with IEEE1394a. Your applications will grow as technical progress advances.

Note

All naming in this document relates to FirePackage, not to GenICam.

Note

For further information on FireWire see FireWire on page 35.

www

For further information on the highlights of Pike types, the Pike family and the whole range of Allied Vision FireWire cameras read the data sheets and brochures on the website of Allied Vision:

https://www.alliedvision.com/en/support/technical-documentation/pike-documentation

Model	Sensor	Picture size (max.) Format_7 Mode_0	Frame rates at full resolution
Pike F-032B, F-032C Pike F-032B, F-032C fiber	ON Semiconductor KAI-0340 CCD, progressive scan Type 1/3	640 (H) × 480 (V)	Up to 208 fps
Pike F-100B, F-100C Pike F-100B, F-100C fiber	ON Semiconductor KAI-1020 CCD, progressive scan Type 2/3	1000 (H) × 1000 (V)	Up to 60 fps
Pike F-145B, F-145C Pike F-145B, F-145C fiber	Sony Semiconductor ICX285 CCD, progressive scan Type 2/3	1388 (H) × 1038 (V)	Up to 30 fps
Pike F-145B, F-145C-15fps Pike F-145B, F-145C-15fps fiber	Sony Semiconductor ICX285 CCD, progressive scan Type 2/3	1388 (H) × 1038 (V)	Up to 16 fps
Pike F-210B Pike F-210B fiber	ON Semiconductor KAI-2093 CCD, progressive scan Type 1	1920 (H) × 1080 (V)	Up to 31 fps
Pike F-421B, F-421C Pike F-421B, F-421C fiber	ON Semiconductor KAI-4022 CCD, progressive scan Type 1.2	2048 (H) × 2048 (V)	Up to 16 fps
Pike F-505B, F-505C Pike F-505B, F-505C fiber	Sony Semiconductor ICX625 CCD, progressive scan Type 2/3	2456 (H) × 2058 (V)	Up to 15 fps
Pike F-1100B, F-1100C Pike F-1100B, F-1100C fiber	ON Semiconductor KAI-11002 CCD, progressive scan Type 35 mm	4008 (H) × 2672 (V)	Single-tap: up to 2.6 fps Dual-tap: up to 4.9 fps
Pike F-1600B, F-1600C Pike F-1600B, F-1600C fiber	ON Semiconductor KAI-16000 CCD, progressive scan Type 35 mm	4872 (H) × 3248 (V)	Single-tap: up to 1.7 fps Dual-tap: up to 3.1 fps

Table 3: Pike models, resolution, and frame rates

Compliance and intended use

Compliance notifications

For customers in Europe:

Allied Vision has demonstrated the fulfillment of the requirements relating to the Pike camera family:

- Directive 2014/30/EU (Electromagnetic compatibility)
- Directive 2011/65/EU, incl. amendment 2015/863/EU (RoHS)
- Directive 2012/19/EU (Waste of Electric and Electronic Equipment, WEEE)

For customers in the USA

United States of America: Supplier Declaration of Conformity

Pike cameras comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. this device must accept any interference received, including interference that may cause undesired operation.

Responsible Party – U.S. Contact Information

Allied Vision Technologies, Inc.
102 Pickering Way – Suite 502
Exton, PA 19341
Tel: +1 978 225 2030

Note: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Class B digital device

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

We caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Avoid electromagnetic interferences

For all power and interface connections, only use shielded cables or cables recommended by Allied Vision.

Camera applications and intended use

General use

- The user is responsible for operating the camera within the specifications that are defined in this document, and within appropriate environmental conditions and technical prerequisites, to ensure trouble-free camera operation.
- The camera is compliant with current data communication standards; however, those standards do not allow for self-monitoring. Thus, the camera cannot be used as a standalone device for security-related monitoring operations.
- The camera is a hardware product. Only when used with appropriate accompanying software, the camera will produce the desired results. The realization of intelligent solutions requires additional software that is suitable to run with the camera.
- The camera is a component, it is neither a complete product, nor is it a ready-made technical solution.
- The camera-supporting software can be obtained and installed separately from the camera. Usage of the software is solely the responsibility of the user.
- The camera must not be opened. For all repair tasks, contact Allied Vision or one of Allied Vision's authorized representatives.
- Observe the intended use. The camera must only be used for purposes that are in conformity with the stated intended use.
- Additionally, refer to the warranty information on the Allied Vision website.

Use in medical devices

The camera provides basic adequacy to be used in medical devices as well, however, is not specially designated for operation in medical devices. When used as part of a medical device, a review of the specific application is necessary. Users who integrate the camera into an application must comply with the rules and regulations concerning medical devices.

Copyright and trademarks

FireWire

Overview

FireWire provides one of the most comprehensive, high-performance, and cost-effective solutions platforms. FireWire offers very impressive throughput at very affordable prices.

Definition

FireWire (also known as i.Link or IEEE1394) is a personal computer and digital video serial bus interface standard, offering high-speed communications and isochronous real-time data services. FireWire has low implementation costs and a simplified and adaptable cabling system.

Figure 1: FireWire Logo

IEEE1394 standards

FireWire was developed by Apple in the late 1990s, after work defining a slower version of the interface by the IEEE1394 working committee in the 1980s. Apple's development was completed in 1995. It is defined in IEEE standard 1394, which is currently a composite of three documents:

- Original IEEE Std. 1394-1995
- IEEE Std. 1394a-2000 amendment
- IEEE Std. 1394b-2002 amendment

FireWire is used to connect digital cameras, especially in industrial systems for machine vision.

Note

All naming in this document relates to FirePackage, not to GenICam.

Why use FireWire?

Digital cameras with on-board FireWire (IEEE1394a or IEEE1394b) communications conforming to the IIDC standard (V1.3 or V1.31) have created cost-effective and powerful solutions options being used for thousands of different applications around the world. FireWire is currently the premier robust digital interface for industrial applications for many reasons, including:

- Guaranteed bandwidth features to ensure fail-safe communications
- Interoperability with multiple different camera types and vendors
- Diverse camera powering options, including single-cable solutions up to 45 W
- Effective multiple-camera solutions
- Large variety of FireWire accessories for industrial applications
- Availability of repeaters and optical fiber cabling
- Forward and backward compatibility blending IEEE1394a and IEEE1394b
- Both real-time (isochronous) and demand-driven asynchronous data transmission capabilities

FireWire in detail

Serial bus

FireWire is a very effective way to utilize a low-cost serial bus, through a standardized communications protocol, that establishes packetized data transfer between two or more devices. FireWire offers real-time isochronous bandwidth for image transfer with guaranteed low latency. It also offers asynchronous data transfer for controlling camera parameters on the fly, such as gain and shutter. As illustrated in the diagram below, these two modes can co-exist by using priority time slots for video data transfer and the remaining time slots for control data transfer.

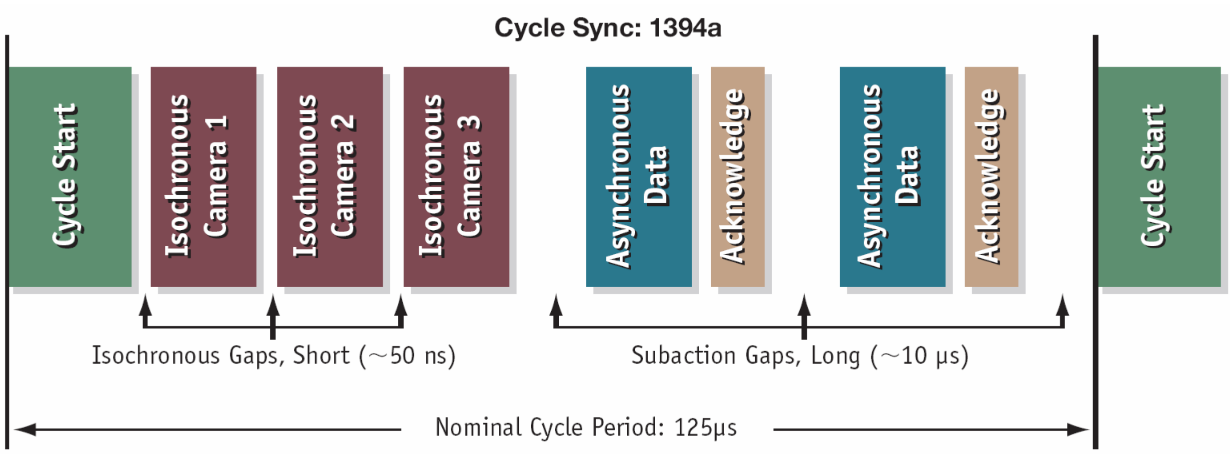


Figure 2: IEEE1394a data transmission

Whereas IEEE1394a works in half duplex transmission, IEEE1394b does full duplex transmission. IEEE1394b optimizes the usage of the bandwidth, as it does not need gaps between the signals like IEEE1394a. This is due to parallel arbitration, handled by the bus owner supervisor selector (BOSS). For details see the following diagram:

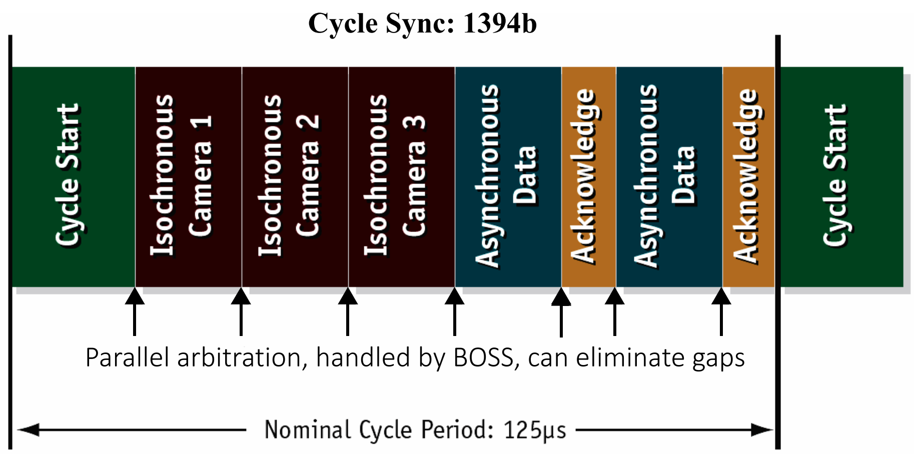


Figure 3: IEEE1394b data transmission

Additional devices may be added up to the overall capacity of the bus, but throughput at guaranteed minimum service levels is maintained for all devices with an acknowledged claim on the bus. This deterministic feature is a huge advantage for many industrial applications where robust performance is required. This applies with applications that do not allow dropping images within a specific time interval.

FireWire connection capabilities

FireWire can connect together up to 63 peripherals in an acyclic network structure (hubs). It allows peer-to-peer device communication between digital cameras, without using system memory or the CPU.

A FireWire camera can directly, via direct memory access (DMA), write into or read from the memory of the computer with almost no CPU load.

FireWire also supports multiple hosts per bus. FireWire requires only a cable with the correct number of pins on either end (normally 6 or 9).

Note

How to extend the size of an isochronous packet up to 11.000 byte at S800:

- see register 0xF1000048, ADV_INQ_3, Max IsoSize [1] in Table 156: Advanced register: Advanced feature inquiry
- see Maximum ISO packet size

Caution

While supplying such an amount of bus power is clearly a beneficial feature, it is very important not to exceed the inrush current of 18 mJoule in 3 ms.

Higher inrush current may damage the PHY chip of the camera and/or the PHY chip in your PC.

Capabilities of IEEE1394a (FireWire 400)

FireWire 400 (S400) is able to transfer data between devices at 100, 200, or 400 MBit/s data rates.

The IEEE1394a capabilities in detail:

- 400 Mbit/s
- Hot-pluggable devices
- Peer-to-peer communications
- Direct Memory Access (DMA) to host memory
- Guaranteed bandwidth
- Multiple devices (up to 45 W) powered via FireWire bus

IIDC V1.3 camera control standards

IIDC V1.3 released a set of camera control standards via IEEE1394a, which established a common communications protocol on which most current FireWire cameras are based.

In addition to common standards shared across manufacturers, Allied Vision offers Format_7 mode that provides special features (smart features), such as:

- Higher resolutions
- Higher frame rates
- Diverse color modes

as extensions (advanced registers) to the prescribed common set.

FireWire 800

FireWire 800 (S800) was introduced commercially by Apple in 2003 and has a 9-pin FireWire 800 connector (see details in the *1394 Installation Manual* and in IEEE1394b port pin assignment). This newer IEEE1394b specification allows a transfer rate of 800 MBit/s with backward compatibility to the slower rates and 6-pin connectors of FireWire 400.

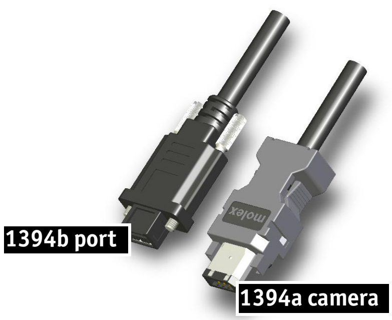
The IEEE1394b capabilities in detail:

- 800 Mbit/s
- All previously described benefits of IEEE1394a
- Interoperability with IEEE1394a devices
- Longer communications distances (up to 500 m using GOF cables)

IIDC V1.31 camera control standards

Along with IEEE1394b, the IIDC V1.31 standard arrived in January 2004, evolving the industry standards for digital imaging communications to include I/O and RS232 handling, and adding further formats. The increased bandwidths enable transmitting high-resolution images to the PC's memory at high frame rates.

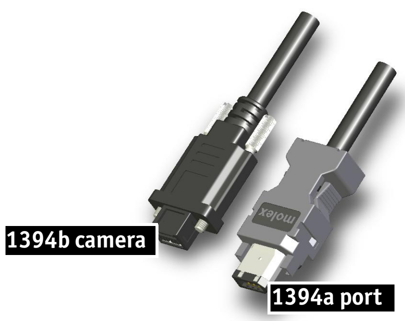
Compatibility between IEEE1394a and IEEE1394b



IEEE1394a camera connected to IEEE1394b bus

The cable explains dual compatibility: This cable serves to connect an IEEE1394a camera with its six-pin connector to a bilingual port (a port which can talk in a- or b-language) of a IEEE1394b bus.

In this case, the b-bus communicates in a-language and a-speed with the camera achieving a-performance



IEEE1394b camera connected to IEEE1394a bus

The cable explains dual compatibility: In this case, the cable connects an IEEE1394b camera with its nine-pin connector to a IEEE1394a port.

In this case, the b-camera communicates in a-language with the camera achieving a-performance

Figure 4: IEEE1394a and IEEE1394b cameras and compatibility

Compatibility example

It is possible to run a IEEE1394a and a IEEE1394b camera on the 1394b bus.

You can e.g. run a Pike F-032B and a Marlin F-033B on the same bus:

- Pike F-032B @ S800 and 120 fps (5120 bytes per cycle, 64% of the cycle slot)
- Marlin F-033B @ S400 and 30 fps (1280 bytes, 32% of the cycle slot)

Bus runs at 800 Mbit/s for all devices. Data from Marlin's port is up-converted from 400 Mbit/s to 800 Mbit/s by data doubling (padding), still needing 32% of the cycle slot time. This doubles the bandwidth requirement for this port, as if the camera were running at 60 fps. Total consumption is thus 5120 + 2560 = 7680 bytes per cycle.

Image transfer via IEEE1394a and IEEE1394b

Technical detail	IEEE1394a	IEEE1394b
Transmission mode	Half duplex (both pairs needed) 400 Mbit/s data rate aka: a-mode, data/strobe (D/S) mode, legacy mode	Full duplex (one pair needed) 1 Gbit/s signaling rate, 800 Mbit/s data rate 10b/8b coding (Ethernet), aka: b-mode (beta mode)
Devices	Up to 63 devices per network	
Number of cameras	Up to 16 cameras per network	
Number of DMAs	4 to 8 DMAs (parallel) cameras / bus	
Real-time capability	Image has real-time priority	
Available bandwidth acc. IIDC (per cycle 125 µs)	4096 bytes per cycle ~ 1000 quadlets @ 400 Mbit/s	8192 bytes per cycle ~ 2000 quadlets @ 800 Mbit/s (@1 GHz clock rate)
	For more information, see Frame rates.	
Max. image bandwidth	31.25 MByte/s	62.5 MByte/s
Max. total bandwidth	~45 MByte/s	~85 MByte/s
Number of busses	Multiple busses per PC limit: PCI bus	Multiple busses per PC limit: PCI (Express) bus
CPU load	Almost none for DMA image transfer	
Gaps	Gaps negatively affect asynchronous performance of widespread network (round trip delay), reducing efficiency	No gaps needed, BOSS mode for parallel arbitration

Table 4: Technical detail comparison: IEEE1394a and IEEE1394b

Note

The bandwidth values refer to 1 MByte = 1024 KB

IEEE1394b bandwidths

According to the IEEE1394b specification on isochronous transfer, the largest recommended data payload size is 8192 bytes per 125 µs cycle at a bandwidth of 800 Mbit/s.

Note

Certain cameras may offer, depending on their settings in combination with the use of FirePackage higher packet sizes.

Consult your local distribution partner's support team, if you require additional information on this feature.

Note

How to extend the size of an isochronous packet up to 11.000 byte at S800:

- See register 0xF1000048, ADV_INQ_3, Max IsoSize [1] in Table 156: Advanced register: Advanced feature inquiry

For further details read How does bandwidth affect the frame rate?.

Requirements for PC and IEEE1394b

Note

For FireWire accessories see https://www.alliedvision.com/en/contact

Caution

As mentioned earlier, it is very important not to exceed an inrush energy of 18 mWs in 3 ms. (This means that a device, when powered via 12 V bus power, must never draw more than 1.5 A, especially in the first 3 ms.)

Higher inrush current may damage the physical interface chip of the camera and/or the PHY chip in your PC.

For a single Stingray camera inrush current may not be a problem. But daisy chaining multiple cameras or supplying bus power via (optional) Hirose power out to circuitry with unknown inrush currents needs careful design considerations.

Example1: IEEE1394b bandwidth of Pike cameras

Pike model	Resolution	Frame rate	Bandwidth
Pike F-032B, F-032C	VGA	208 fps	62.5 MByte/s
Pike F-100B, F-100C	1 megapixel	60 fps	57.6 MByte/s
Pike F-145B, F-145C	1.4 megapixel	30 fps	41.4 MByte/s
Pike F-210B	2.1 megapixel	31 fps	62.5 MByte/s
Pike F-421B, F-421C	4 megapixel	15 fps	62.5 MByte/s
Pike F-505B, F-505C	5 megapixel	13 fps	62.5 MByte/s

Table 5: Pike model bandwidth

Pike model	Resolution	Frame rate	Bandwidth
Pike F-1100B, F-1100C	10.7 megapixel	2.6 fps (single-tap) 4.9 fps (dual-tap)	26.6 MByte/s 50.0 MByte/s
Pike F-1600B, F-1600C	15.8 megapixel	1.7 fps (single-tap) 3.1 fps (dual-tap)	25.7 MByte/s 46.8 MByte/s

Table 5: Pike model bandwidth (continued)

Note

All data are calculated using Raw8 / Mono8 color mode. Higher bit depths or color modes will double or triple bandwidth requirements.

Example 2: More than one Pike camera at full speed

Due to the fact that one Pike camera can, depending on its settings, saturate a 32-bit PCI bus, you are advised to use either a PCI Express card and/or multiple 64-bit PCI bus cards, if you want to use 2 or more Pike cameras simultaneously (see the following table).

Number of cameras	PC hardware required
One Pike camera at full speed	1 × 32-bit PCI bus card (85 MByte/s)
Two or more Pike cameras at full speed	PCI Express card and/or Multiple 64-bit PCI bus cards

Table 6: Required hardware for multiple camera applications

FireWire Plug & play capabilities

FireWire devices implement the ISO/IEC 13213 configuration ROM model for device configuration and identification to provide plug & play capability. All FireWire devices are identified by an IEEE EUI-64 unique identifier (an extension of the 48-bit Ethernet MAC address format) in addition to well-known codes indicating the type of device and protocols it supports. For further details read Configuration of the camera.

FireWire hot-plug and screw-lock precautions

Caution

Hot-plug precautions

- Although FireWire devices can theoretically be hot-plugged without powering down equipment. Allied Vision strongly recommends turning off the computer power, before connecting a digital camera to it.
- Static electricity or slight plug misalignment during insertion may short-circuit and damage components.
- The physical ports may be damaged by excessive electrostatic discharge (ESD), when connected under powered conditions. It is good practice to ensure proper grounding of computer case and camera case to the same ground potential, before plugging the camera cable into the port of the computer. This ensures that no excessive difference of electrical potential exists between computer and camera.
- As mentioned earlier, it is very important not to exceed the inrush energy of 18 mWs in 3 ms. (This means that a device, when powered via 12 V bus power, must never draw more than 1.5 A, especially in the first 3 ms.)
- Higher inrush current may damage the physical interface chip of the camera and/or the PHY chip in your PC.
  For a single Stingray camera inrush current may not be a problem. But daisy chaining multiple cameras or supplying bus power via (optional) Hirose power out to circuitry with unknown inrush currents needs careful design considerations.

Screw-lock precautions

- All Allied Vision IEEE1394b cameras and cables have industrial screw-lock fasteners to insure a tight electrical connection that is resistant to vibration and gravity.
- Allied Vision strongly recommends using only IEEE1394b adapter cards with screw-locks.

Operating system support

Operating system	IEEE1394a	IEEE1394b
Linux	Full support	Full support
Apple Mac OS	Full support	Full support
Microsoft Windows XP	Full support	With SP3 the default speed for IEEE1394b is S100 (100 Mbit/s). A download and registry modification is available from Microsoft to restore performance to either S400 or S800. Note: The Windows IEEE1394 driver only supports IEEE1394a. For IEEE1394b use either the FirePackage or install the driver provided with the IEEE1394 Bus Driver Package. (Both drivers replace the Microsoft OHCI IEEE1394 driver, but the second is 100% compliant to the driver of Microsoft. This way, applications using the MS1394 driver will continue to work.)
Microsoft Windows Vista	Full support	Windows Vista including SP1/SP2 supports IEEE1394b only with S400. Note: The Windows IEEE1394 driver only supports IEEE1394a. For IEEE1394b use either the FirePackage or install the driver provided with the IEEE1394 Bus Driver Package. (Both drivers replace the Microsoft OHCI IEEE1394 driver, but the second is 100% compliant to the driver of Microsoft. This way, applications using the MS1394 driver will continue to work.)
Microsoft Windows 7	Full support	Full support
Microsoft Windows 8	Full support	Full support

Table 7: FireWire and operating system support

www

For more information see Allied Vision Software:
https://www.alliedvision.com

Specifications

Note

- For information on bit/pixel and byte/pixel for each color mode see Table 132: ByteDepth on page 254.
- Maximum protrusion means the distance from lens flange to the glass filter in the camera.

Pike F-032B, F-032C (fiber)

Feature	Specification
Image device	ON Semiconductor KAI-0340 with HAD microlens CCD, progressive scan Type 1/3 (5.92 mm diagonal)
Effective chip size	4.7 mm × 3.6 mm
Cell size	7.4 µm × 7.4 µm
Picture size (max.)	640 × 480 pixels (Format_7 Mode_0)
Lens mount	Adjustable C-Mount: 17.526 mm (in air); Ø 25.4 mm (32 tpi) mechanical flange back to filter distance: 12.5 mm (see Figure 16: C-Mount cross section (VGA size filter) on page 70)
ADC	14-bit
Color modes	Pike F-032C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 15 fps; 30 fps; 60 fps; 120 fps up to 208 fps in Format_7 (Mono8)
Gain control	Manual: 0 to 22 dB (0.0353 dB/step); auto gain (select. AOI)
Shutter speed	18 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 105 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)

Table 8: Pike F-032B, F-032C (fiber) model specification

Feature	Specification
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 64 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-032C: Auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose
Power consumption	Typical 5 W @ 12 VDC Fiber: typical 5.75 W @ 12 VDC (@ full resolution and maximum frame rate)
Dimensions (L × W × H)	96.8 × 44 × 44 mm
Mass (typical)	250 g
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-032B: protection glass Pike F-032C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 8: Pike F-032B, F-032C (fiber) model specification (continued)

Pike F-100B, F-100C (fiber)

Feature	Specification
Image device	ON Semiconductor KAI-1020 with HAD microlens CCD, progressive scan Type 2/3 (10.5 mm diagonal)
Effective chip size	7.4 mm × 7.4 mm
Cell size	7.4 µm × 7.4 µm
Picture size (max.)	1000 × 1000 pixels (Format_7 Mode_0)
Lens mount	Adjustable C-Mount: 17.526 mm (in air); Ø 25.4 mm (32 tpi) mechanical flange back to filter distance: 12.5 mm (see Figure 17: C-Mount cross section (large filter) on page 71)
ADC	14-bit
Color modes	Pike F-100C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 15 fps; 30 fps; 60 fps up to 60 fps in Format_7 (Mono8)
Gain control	Manual: 0 to 22 dB (0.0353 dB/step); auto gain (select. AOI)
Shutter speed	43 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 32 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 64 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-100C: auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose
Power consumption	Typical 5 W @ 12 VDC Fiber: typical 5.75 W @ 12 VDC
Dimensions (L × W × H)	96.8 × 44 × 44 mm
Mass (typical)	250 g

Table 9: Pike F-100B, F-100C (fiber) model specifications

Feature	Specification
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-100B: protection glass Pike F-100C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 9: Pike F-100B, F-100C (fiber) model specifications (continued)

Pike F-145B, F-145C (fiber) (-15fps*)

* Variant: F-145-15fps only

This variant offers lower speed (only 15 fps), but better image quality.

Feature	Specification
Image device	Sony Semiconductor ICX285 with EXview HAD microlens CCD, progressive scan Type 2/3 (11.2 mm diagonal)
Effective chip size	9.0 mm × 6.7 mm
Cell size	6.45 µm × 6.45 µm
Picture size (max.)	1388 × 1038 pixels (Format_7 Mode_0)
Lens mount	Adjustable C-Mount: 17.526 mm (in air); Ø 25.4 mm (32 tpi) mechanical flange back to filter distance: 12.5 mm (see Figure 16: C-Mount cross section (VGA size filter) on page 70)
ADC	14-bit
Color modes	Pike F-145C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 15 fps; 30 fps (* Variant: F-145-15fps only up to 15 fps) up to 30 (16*) fps in Format_7 (Mono8/12 no sub-sampling)
Gain control	Manual: 0 to 32 dB (0.0358 dB/step); auto gain (select. AOI)
Shutter speed	39 (71*) µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 22 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 64 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-145C: Auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose

Table 10: Pike F-145B, F-145C (fiber) model specifications

Feature	Specification
Power consumption	Typical 5 W @ 12 VDC Fiber: typical 5.75 W @ 12 VDC
Dimensions (L × W × H)	96.8 × 44 × 44 mm
Mass (typical)	250 g
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-145B: protection glass Pike F-145C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 10: Pike F-145B, F-145C (fiber) model specifications (continued)

Pike F-210B (fiber)

Feature	Specification
Image device	ON Semiconductor KAI-2093 with HAD microlens CCD, progressive scan Type 1 (16.3 mm diagonal)
Effective chip size	14 mm × 8.0 mm
Cell size	7.4 µm × 7.4 µm
Picture size (max.)	1920 × 1080 pixels (Format_7 Mode_0)
Lens mount	Adjustable C-Mount: 17.526 mm (in air); Ø 25.4 mm (32 tpi) mechanical flange back to filter distance: 12.5 mm (see Figure 17: C-Mount cross section (large filter) on page 71)
ADC	14-bit
Monochrome modes	Mono8, Mono12, Mono16
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 15 fps; 30 fps up to 31 fps in Format_7 (Mono8, no sub-sampling)
Gain control	Manual: 0 to 22 dB (0.0353 dB/step); auto gain (select. AOI)
Shutter speed	43 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External Trigger Shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 15 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 64 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose
Power consumption	Typical 5.5 W @ 12 VDC Fiber: typical 6.25 W @ 12 VDC
Dimensions (L × W × H)	96.8 × 44 × 44 mm
Mass (typical)	250 g
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)

Table 11: Pike F-210B (fiber) model specifications

Feature	Specification
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-210B: protection glass
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 11: Pike F-210B (fiber) model specifications (continued)

Pike F-421B, F-421C (fiber)

Feature	Specification
Image device	ON Semiconductor KAI-04022 with HAD microlens CCD, progressive scan Type 1.2 (21.4 mm diagonal)
Effective chip size	15 mm × 15 mm
Cell size	7.4 µm × 7.4 µm
Picture size (max.)	2048 × 2048 pixels (Format_7 Mode_0)
Lens mount	Adjustable C-Mount: 17.526 mm (in air); Ø 25.4 mm (32 tpi) mechanical flange back to filter distance: 12.5 mm (see Figure 17: C-Mount cross section (large filter) on page 71)
ADC	14-bit
Color modes	Pike F-421C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 15 fps; 30 fps up to 16 fps in Format_7 (Mono8)
Gain control	Manual: 0 to 22 dB (0.0353 dB/step); auto gain (select. AOI)
Shutter speed	70 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 6 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 64 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-421C: Auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose
Power consumption	Typical 5.5 W @ 12 VDC Fiber: typical 6.25 W @ 12 VDC
Dimensions (L × W × H)	96.8 × 44 × 44 mm
Mass (typical)	250 g

Table 12: Pike F-421B, F-421C (fiber) model specifications

Feature	Specification
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-421B: protection glass Pike F-421C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 12: Pike F-421B, F-421C (fiber) model specifications (continued)

Pike F-505B, F-505C (fiber)

Feature	Specification
Image device	Sony Semiconductor ICX625 with Super HAD microlens CCD, progressive scan Type 2/3 (11.0 mm diagonal)
Effective chip size	8.5 mm × 7.1 mm
Cell size	3.45 µm × 3.45 µm
Picture size (max.)	2452 × 2054 pixels (Format_7 Mode_0)
Lens mount	Adjustable C-Mount: 17.526 mm (in air); Ø 25.4 mm (32 tpi) mechanical flange back to filter distance: 12.5 mm (see Figure 17: C-Mount cross section (large filter) on page 71)
ADC	14-bit
Color modes	Pike F-505C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 13 fps up to 14* fps in Format_7 (Mono8 no sub-sampling) * at 11000 bytes per packet
Gain control	Manual: 0 to 24 dB (0.0359 dB/step); auto gain (select. AOI)
Shutter speed	27 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 5 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 64 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-505C: Auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose
Power consumption	Typical 5.75 W @ 12 VDC Fiber: typical 6.50 W @ 12 VDC
Dimensions (L × W × H)	96.8 × 44 × 44 mm

Table 13: Pike F-505B, F-505C (fiber) model specifications

Feature	Specification
Mass (typical)	250 g
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-505B: protection glass Pike F-505C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 13: Pike F-505B, F-505C (fiber) model specifications (continued)

Pike F-1100B, F-1100C (fiber)

Feature	Specification
Image device	ON Semiconductor KAI-11002 with Super HAD microlens CCD, progressive scan Type 35 mm (43.3 mm diagonal)
Effective chip size	37.25 mm × 25.7 mm
Cell size	9.0 µm × 9.0 µm
Picture size (max.)	4008 × 2672 pixels
Lens mount	Standard: F-Mount: 46.5 mm (in air) Maximum protrusion: 26 mm (see Figure 22: F-Mount cross section (Pike F-1100 and Pike F-1600) on page 76))
ADC	14-bit
Color modes	Pike F-1100C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps up to 2.6* fps (single-tap) / up to 4.9* fps (dual-tap) in Format_7 (Mono8 no sub-sampling) * at 11000 bytes per packet User can switch between single-tap and dual-tap.
Gain control	Manual: 0 to 24 dB (0.0359 dB/step); auto gain (select. AOI)
Shutter speed	129 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 5 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 256 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-1100C: Auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose

Table 14: Pike F-1100B, F-1100C (fiber) model specifications

Feature	Specification
Power consumption	Typical single-tap: 5 W @ 12 VDC Fiber: typical 5.5 W @ 12 VDC Typical dual-tap: 5.5 W @ 12 VDC fiber: typical 6.0 W @ 12 VDC
Dimensions (L × W × H)	142.8 × 59 × 59 mm
Mass (typical)	380 g
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-1100B: protection glass Pike F-1100C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 14: Pike F-1100B, F-1100C (fiber) model specifications (continued)

Pike F-1600B, F-1600C (fiber)

Feature	Specification
Image device	ON Semiconductor KAI-16000 with Super HAD microlens CCD, progressive scan Type 35 mm (43.3 mm diagonal)
Effective chip size	36.1 mm × 24 mm
Cell size	7.4 µm × 7.4 µm
Picture size (max.)	4872 × 3248 pixels
Lens mount	Standard: F-Mount: 46.5 mm (in air) Maximum protrusion: 26 mm (see Figure 22: F-Mount cross section (Pike F-1100 and Pike F-1600) on page 76))
ADC	14-bit
Color modes	Pike F-1600C: Raw8, Raw12, Raw16, Mono8, YUV422, YUV411, RGB8
Frame rates	1.875 fps; 3.75 fps; 7.5 fps; 15 fps up to 1.7* fps (single-tap) / up to 3.1* fps (dual-tap) in Format_7 (Mono8 no sub-sampling) * at 11000 bytes per packet User can switch between single-tap and dual-tap.
Gain control	Manual: 0 to 24 dB (0.0359 dB/step); auto gain (select. AOI)
Shutter speed	636 µs to 67,108,864 µs (~67s); auto shutter (select. AOI)
External trigger shutter	Programmable, trigger level control, single trigger, bulk trigger, programmable trigger delay
Image buffer	Up to 5 frames
Look-up tables	16 user-defined (14-bit → 14-bit); gamma (0.45 and 0.7)
Smart functions	Auto gain control (AGC), auto exposure control (AEC), real-time shading correction, Look-up table (LUT), 256 MByte image memory, mirror, binning, sub-sampling, High SNR, storable user sets Pike F-1600C: Auto white balance (AWB), color correction, hue, saturation, sharpness Two configurable inputs, four configurable outputs RS232 port (serial port, IIDC V1.31)
Transfer rate	100 Mbit/s, 200 Mbit/s, 400 Mbit/s, 800 Mbit/s
Digital interface	IEEE1394b (IIDC V1.31), 2 × copper connectors (bilingual) (daisy chain) Fiber: IEEE1394b, 2 connectors: 1 × copper (bilingual), 1 × GOF connector (2 × optical fiber on LCLC), (daisy chain)
Power requirements	DC 8 V to 36 V via IEEE1394 cable or 12-pin Hirose

Table 15: Pike F-1600B, F-1600C (fiber) model specifications

Feature	Specification
Power consumption	Typical single-tap: 6.25 W @ 12 VDC fiber: typical 6.75 W @ 12 VDC Typical dual-tap: 6.5 W @ 12 VDC fiber: typical 7.0 W @ 12 VDC
Dimensions (L × W × H)	142.8 × 59 × 59 mm
Mass (typical)	380 g
Operating temperature	+ 5 °C to + 50 °C housing temperature (without condensation)
Storage temperature	- 10 °C to + 70 °C ambient temperature (without condensation)
Regulations	CE: 2014/30/EU (EMC), 2011/65/EU (RoHS); FCC Class B
Standard accessories	Pike F-1600B: protection glass Pike F-1600C: IR cut filter
Software packages	https://www.alliedvision.com/en/support/software-downloads

Table 15: Pike F-1600B, F-1600C (fiber) model specifications (continued)

Absolute QE

Note

All measurements were done without protection glass or without filter.

The uncertainty in measurement of the QE values is ±10.25%.

This is mainly due to:

- Manufacturing tolerance of the sensor
- Uncertainties in the measuring apparatus itself

Pike F-032B, F-032C

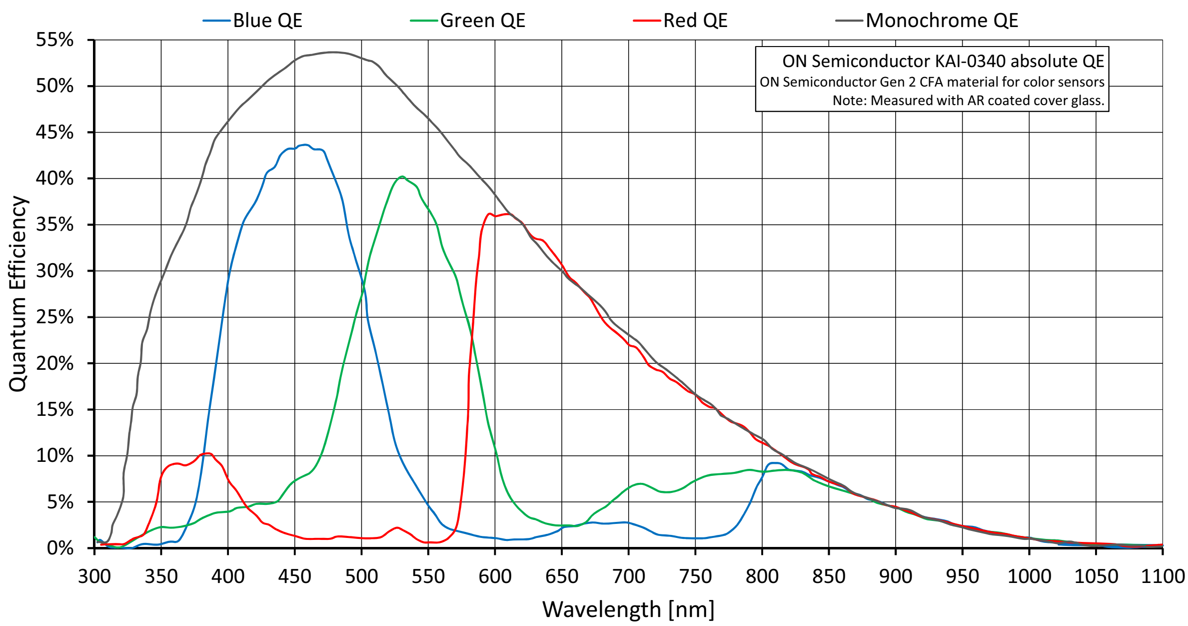


Figure 5: Pike F-032B, F-032C (ON Semiconductor KAI-0340) absolute QE

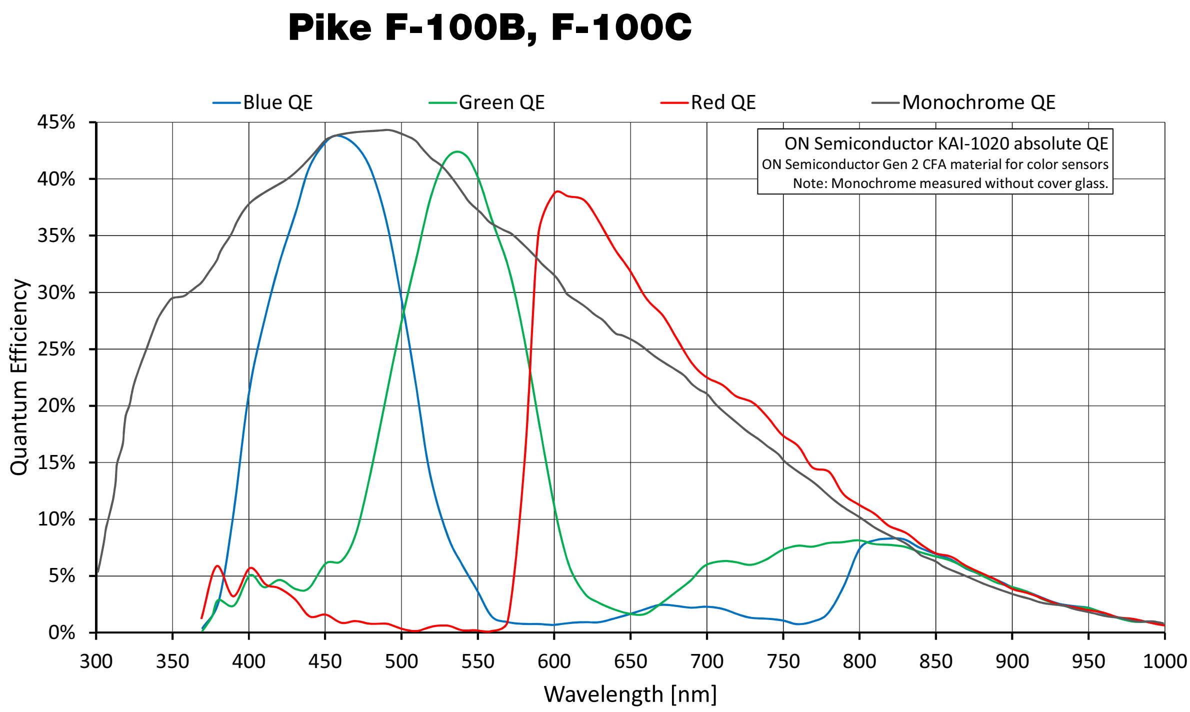


Figure 6: Pike F-100B, F-100C (ON Semiconductor KAI-1020) absolute QE

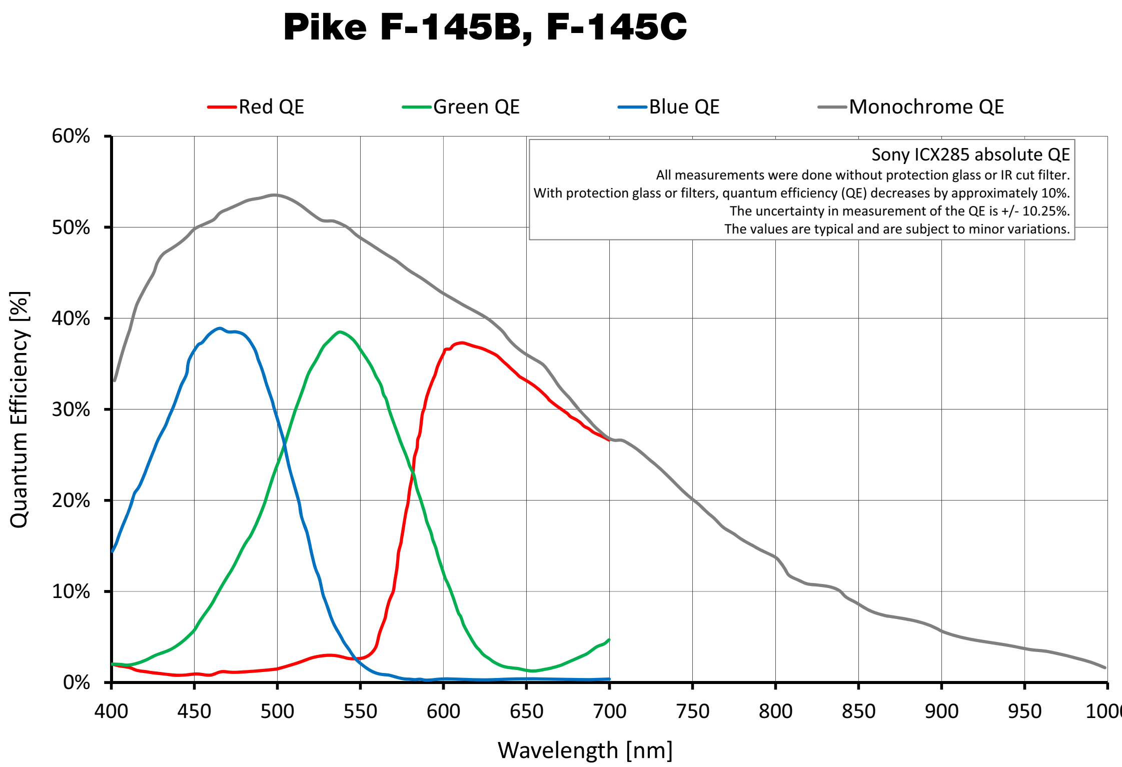


Figure 7: Pike F-145B, F-145C (Sony Semiconductor ICX285) absolute QE

Pike F-210B

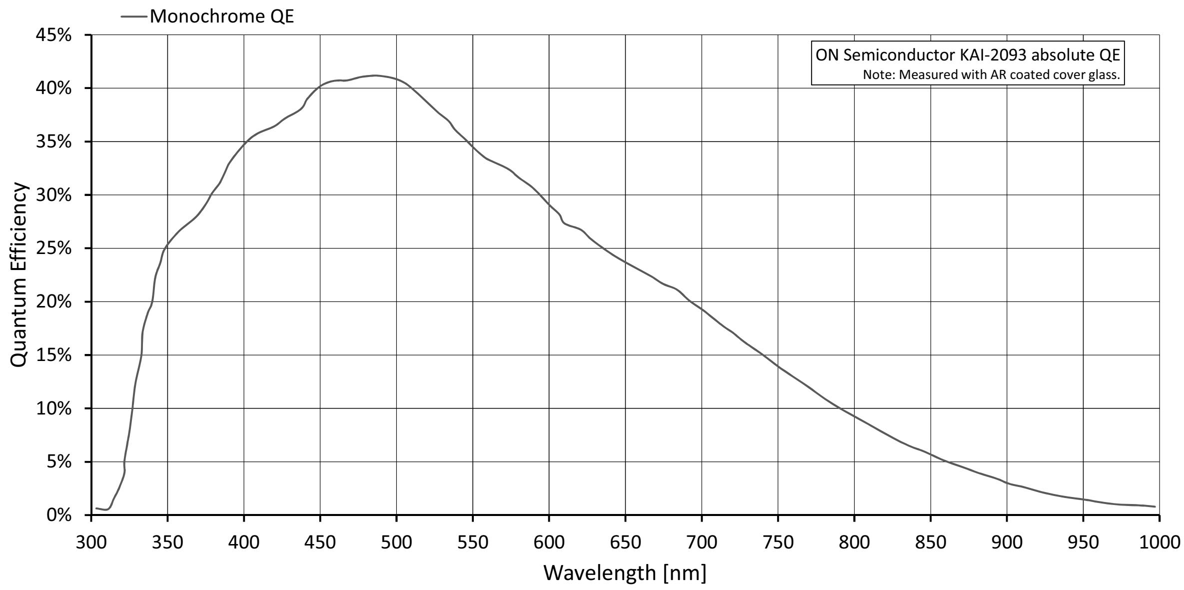


Figure 8: Pike F-210B (ON Semiconductor KAI-02093) absolute QE

Pike F-421B, F-421C

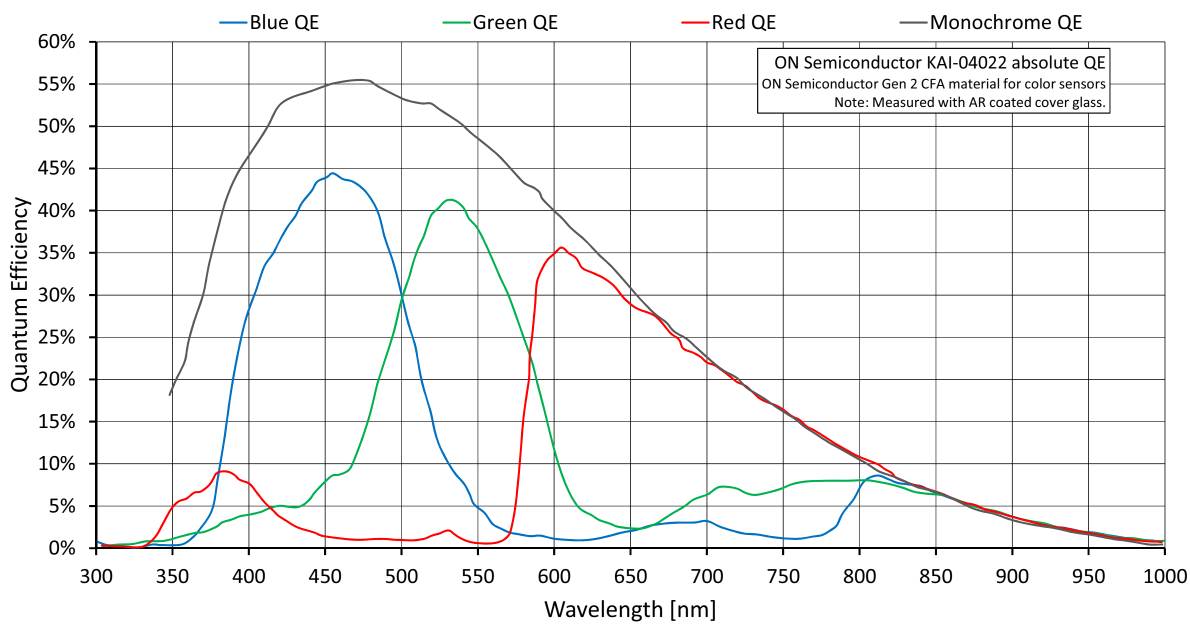


Figure 9: Pike F-421B, F-421C (ON Semiconductor KAI-04022) absolute QE

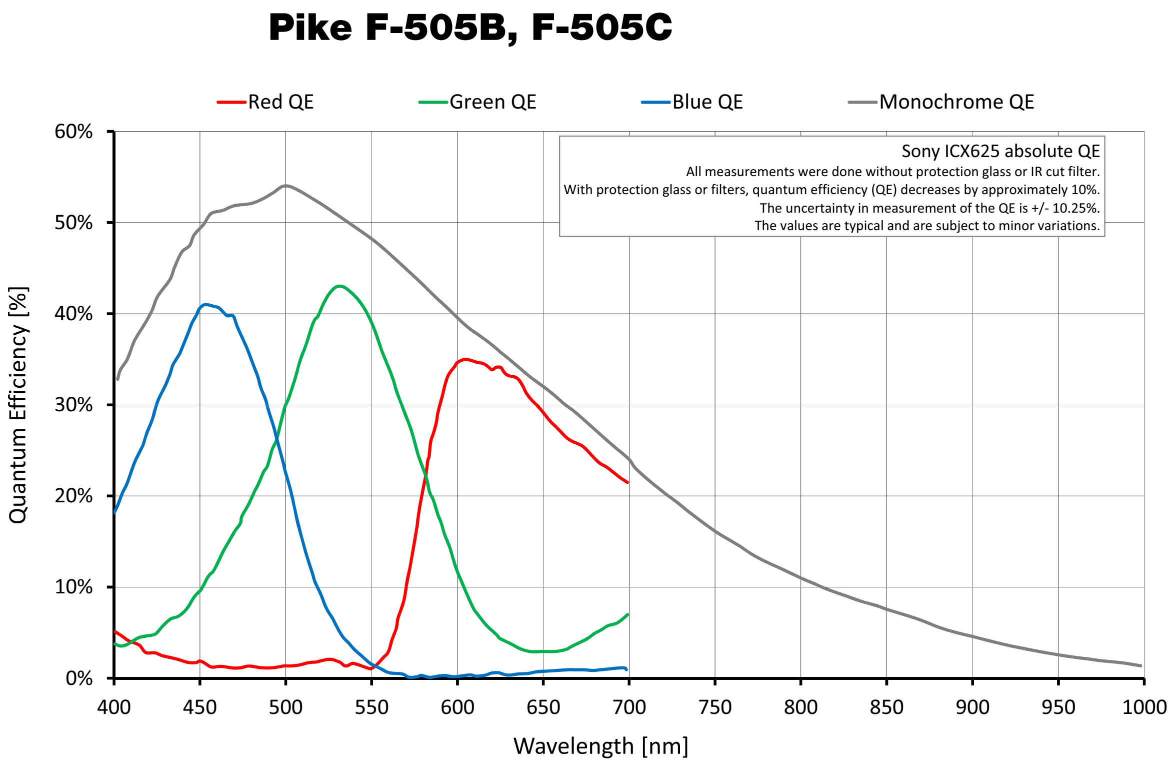


Figure 10: Pike F-505B, F-505C (Sony Semiconductor ICX625) absolute QE

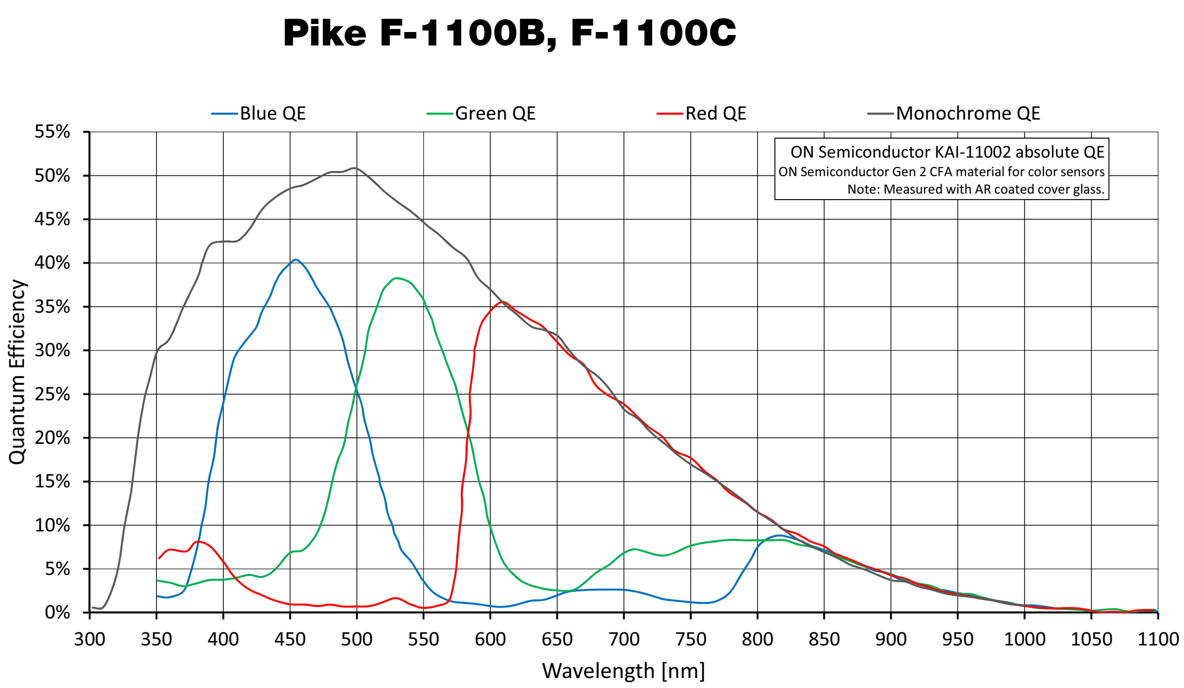


Figure 11: Pike F-1100B, F-1100C (ON Semiconductor KAI-11002) absolute QE

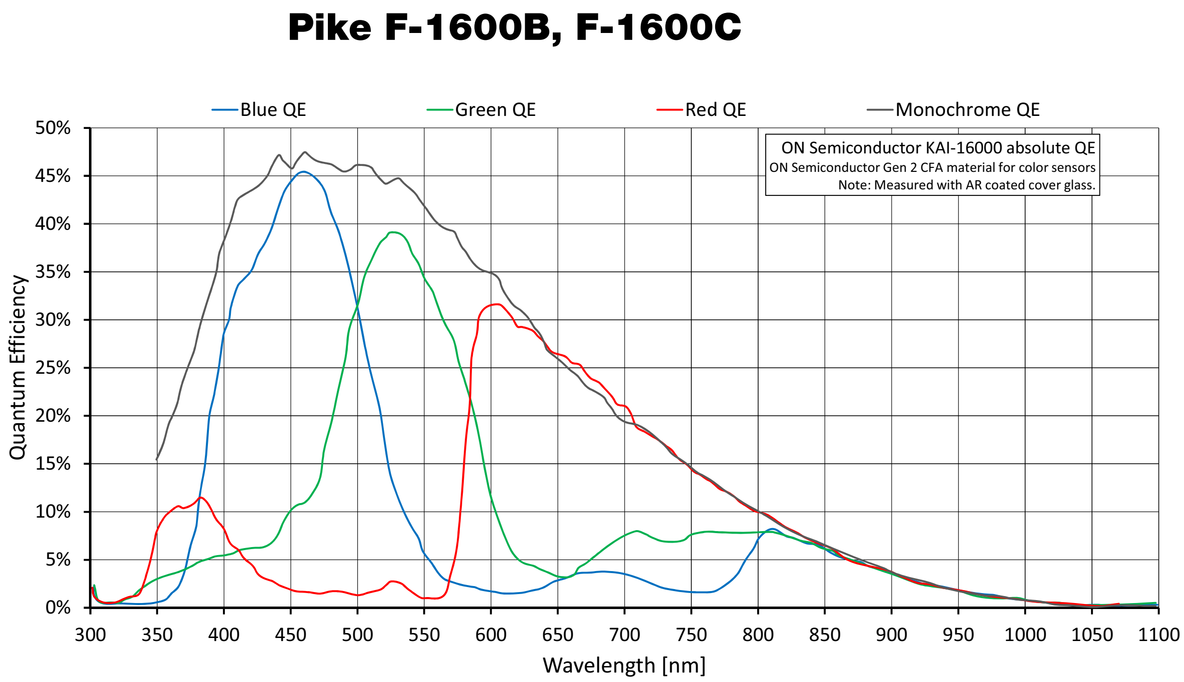


Figure 12: Pike F-1600B, F-1600C (ON Semiconductor KAI-16000) absolute QE

Camera dimensions

Note

For information on sensor position accuracy:

(sensor shift x/y, optical back focal length z and sensor rotation α) see Sensor position accuracy.

Serial numbers for new front flange

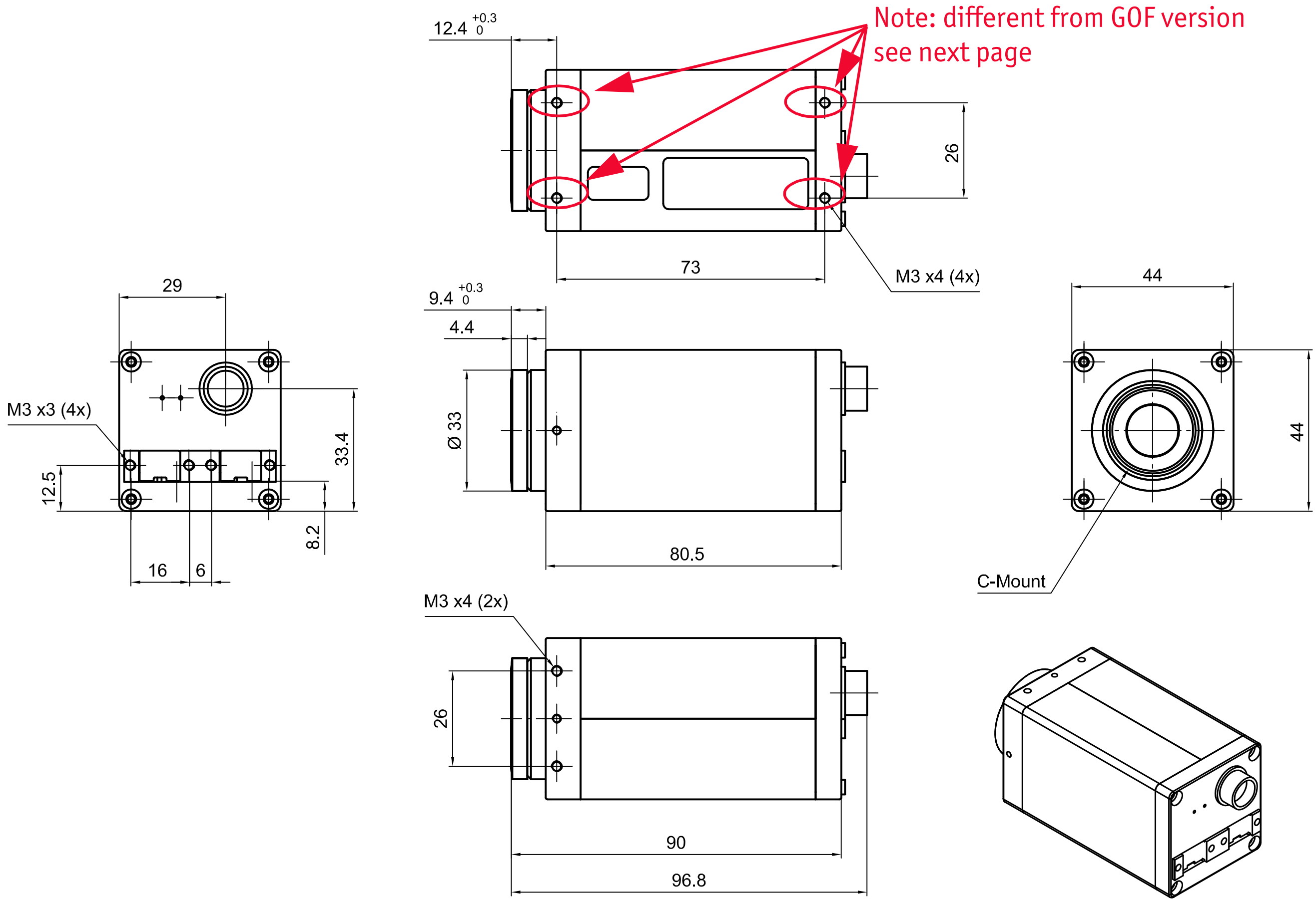
Camera model	E-number	Serial number
Pike F-421B	E0000882	... from SN: 09/16-269066321
Pike F-505B	E0001141	... from SN: 09/16-269066246

Table 16: Starting serial numbers for new front flange

C-Mount

Standard housing dimensions

Interface: 2 × copper

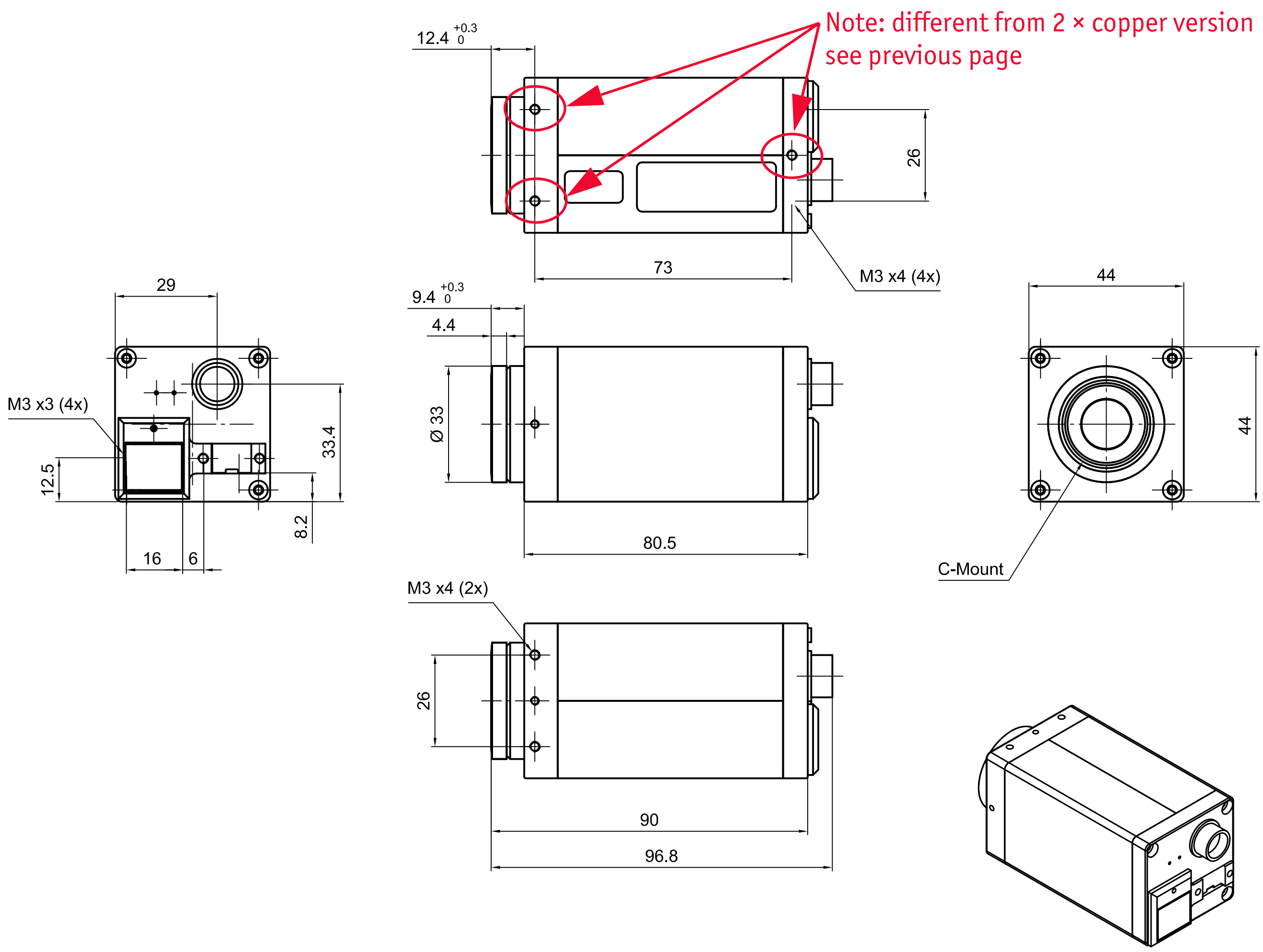


Body size: 96.8 × 44 × 44 mm (L × W × H)

Mass: 250 g (without lens)

Figure 13: Standard housing dimensions (C-Mount, 2 × copper)

Interface: 1 × GOF, 1 × copper



Body size: 96.8 × 44 × 44 mm (L × W × H)

Mass: 250 g (without lens)

Figure 14: Standard housing dimensions (C-Mount, 1 × GOF, 1 × copper)

Tripod adapter dimensions

This tripod adapter is designed for C-Mount standard housings.

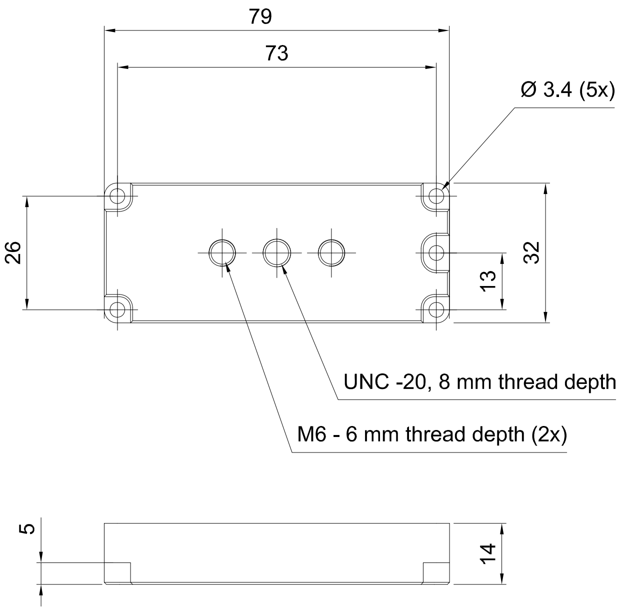


Figure 15: Tripod dimensions (C-Mount)

Cross section: C-Mount (VGA size filter)

Pike F-032, F-100, F-145, F-505 cameras are equipped with VGA size filter.

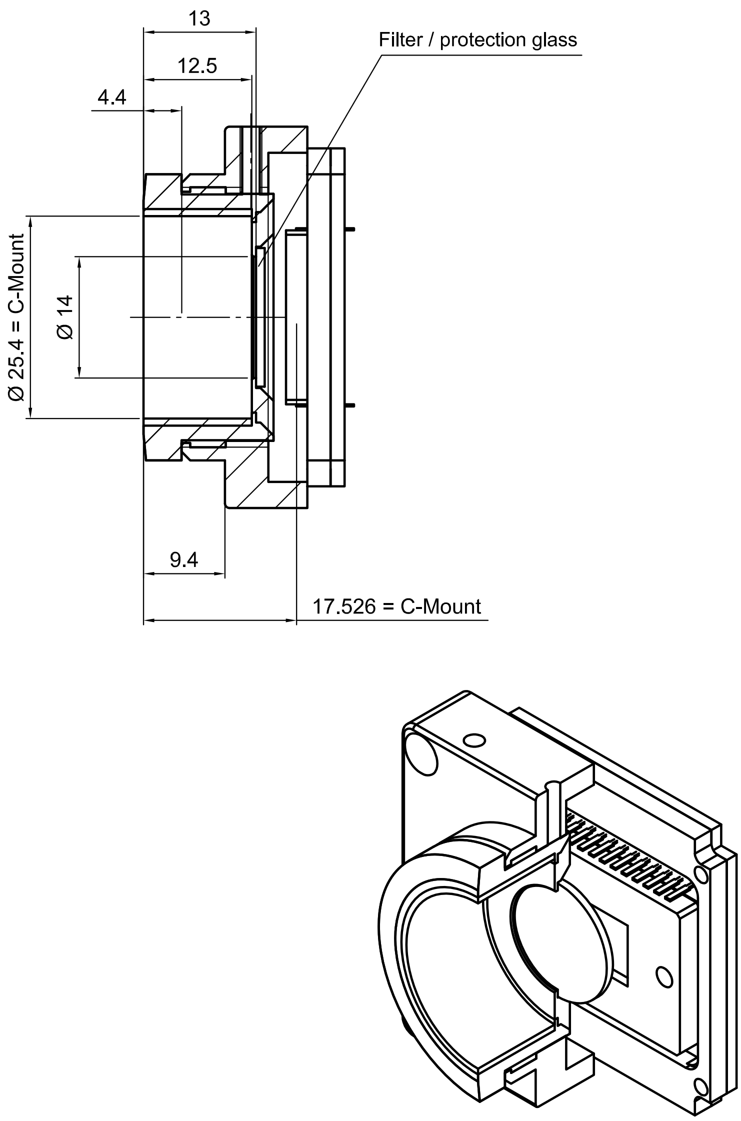
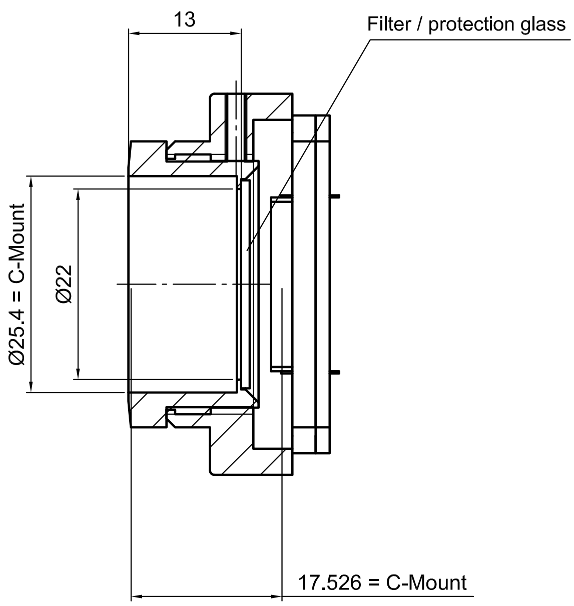


Figure 16: C-Mount cross section (VGA size filter)

Cross section: C-Mount (large filter)

Pike F-210, F-421 are equipped with a large filter.



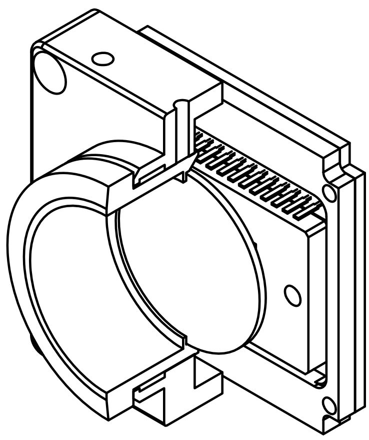


Figure 17: C-Mount cross section (large filter)

C-Mount adjustment

Pike cameras allow the precise adjustment of the back focus of the C-Mount by means of a back focus ring which is threaded into the C-Mount and held by two screws: one on the top (middle) and one on the right side of the camera. The mechanical adjustment of the imaging device is important in order to achieve a perfect alignment with the focal point of the lens.

Individual adjustment may be required:

- if you cannot focus correctly at near or far distances or
- if the back focal plane of your lens does not conform to the C-Mount back-focus specification or
- if you have e.g. removed the IR cut filter.

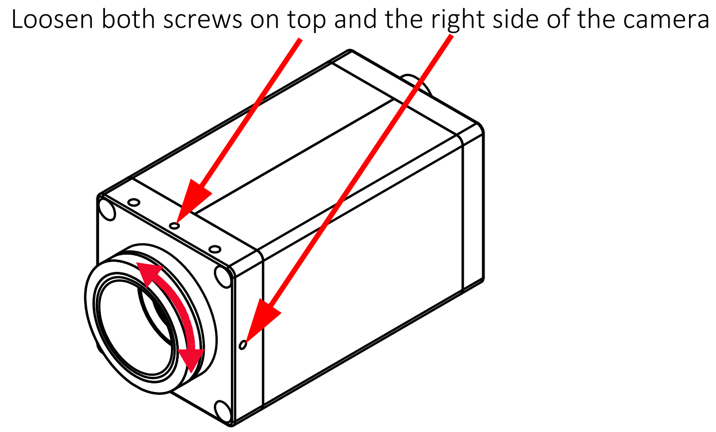


Figure 18: Back focus adjustment

Do the following:

1. Looking in front of the lens loosen both screws on the top (middle) and the right side of the housing (locations as shown above by arrows) with an Allen key (1.3 × 50; order code: K 9020411).
2. With the lens set to infinity or a known focus distance, set the camera to view an object located at *infinity* or the known distance.
3. Rotate the C-Mount ring and lens forward or backwards on its thread until the object is in sharp focus. Be careful that the lens remains seated in the C-Mount.
4. Once focus is achieved, tighten the two locking screws without applying excessive torque.

F-Mount

Standard housing dimensions

Interface: 2 × copper

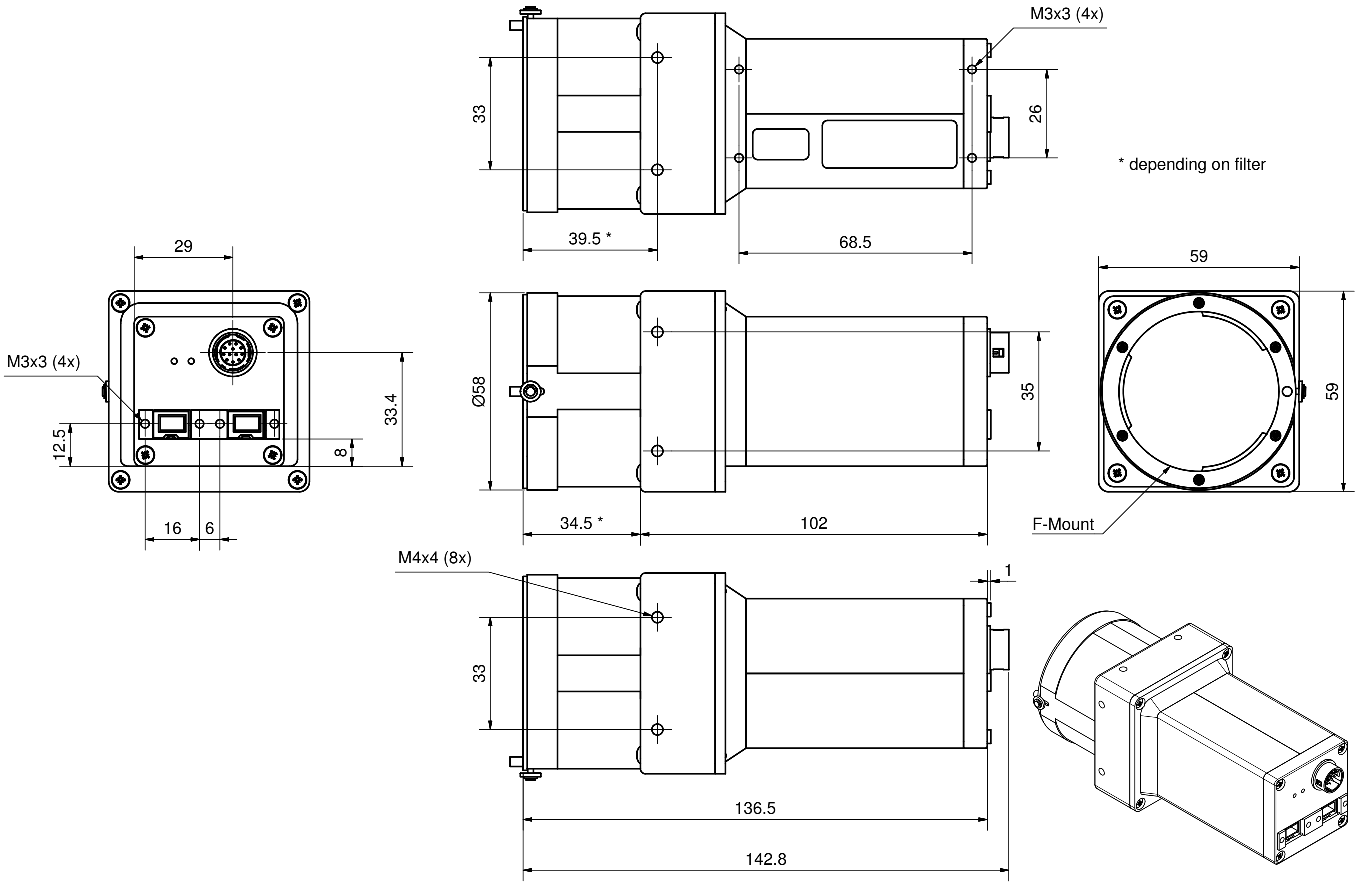


Figure 19: Standard housing (F-Mount, 2 × copper)

Interface: 1 × GOF, 1 × copper

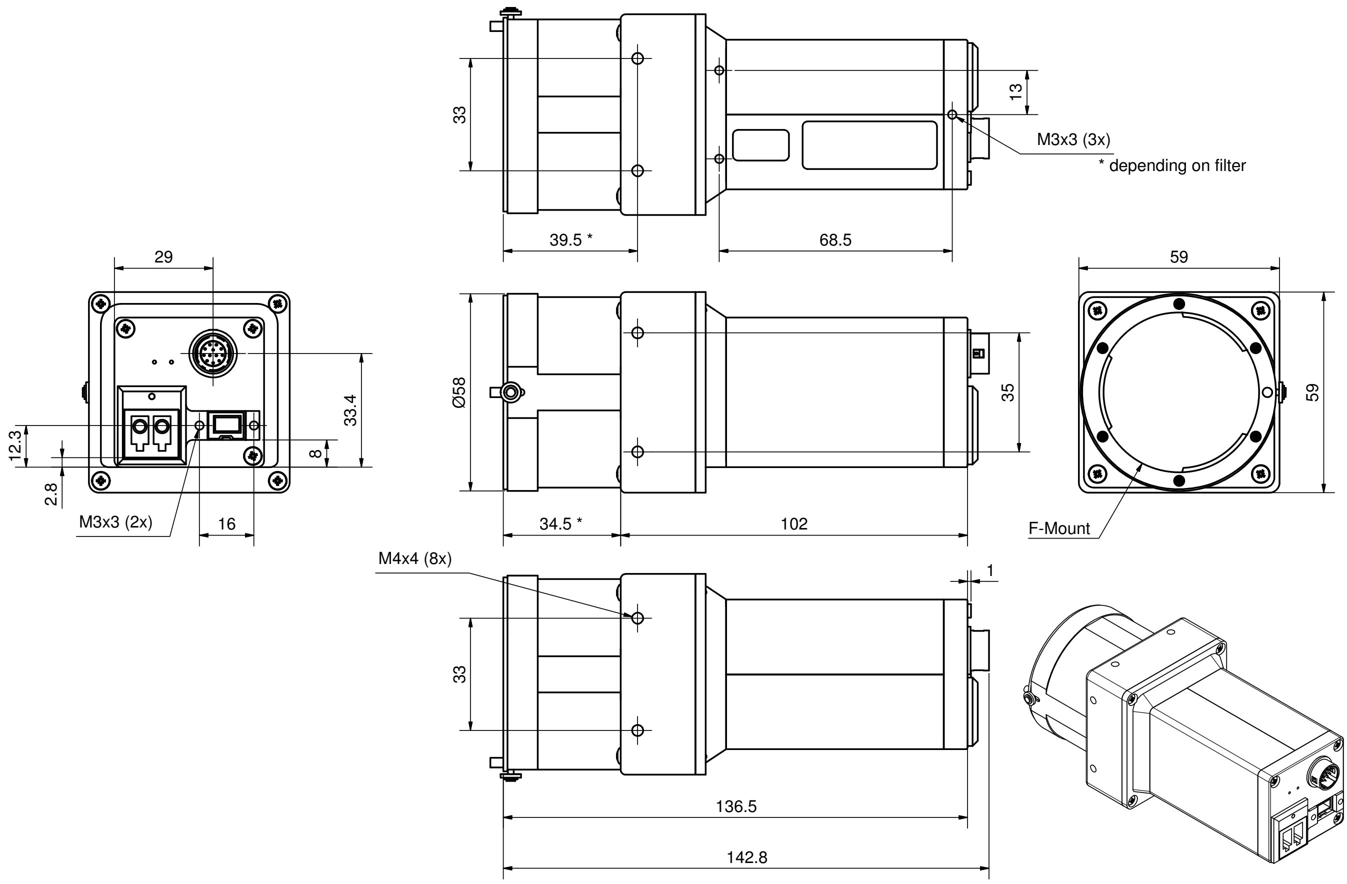


Figure 20: Standard housing (F-Mount, 1 × GOF, 1 × copper)

Tripod adapter dimensions

This tripod adapter is designed for Pike F-Mount standard housings.

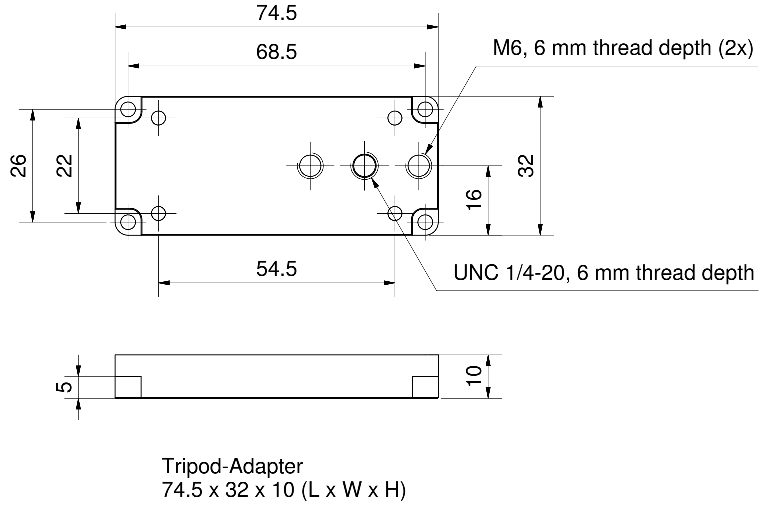


Figure 21: Tripod dimensions (F-Mount)

Cross section

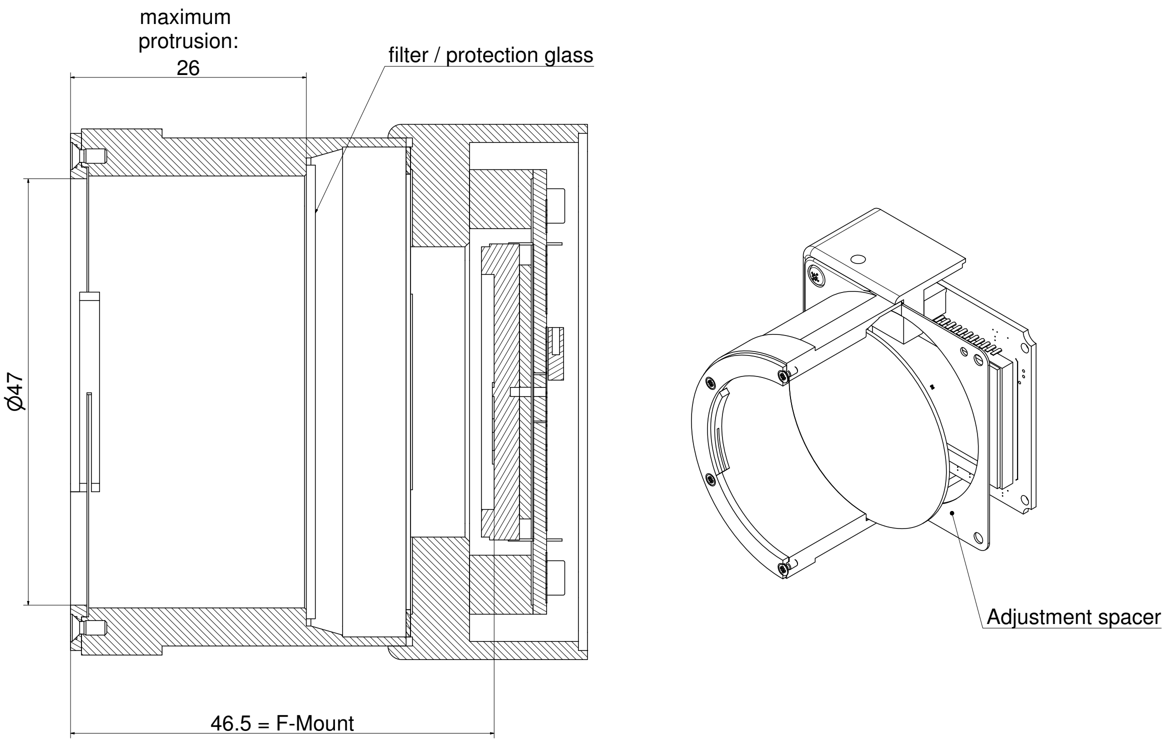


Figure 22: F-Mount cross section (Pike F-1100 and Pike F-1600)

F-Mount adjustment for Pike F-1100 and Pike F-1600

Different from the other Pike cameras Pike: F-1100, F-1600 have built-in filter that cannot be removed.

The dimensional adjustment cannot be done by the customer. All adjustments have to be done by the Allied Vision factory.

If you need any adjustments, please contact Customer Care: For phone numbers and e-mail, see Contacting Allied Vision.

Filter and lenses

IR cut filter: spectral transmission

The following illustration shows the spectral transmission of the IR cut filter.

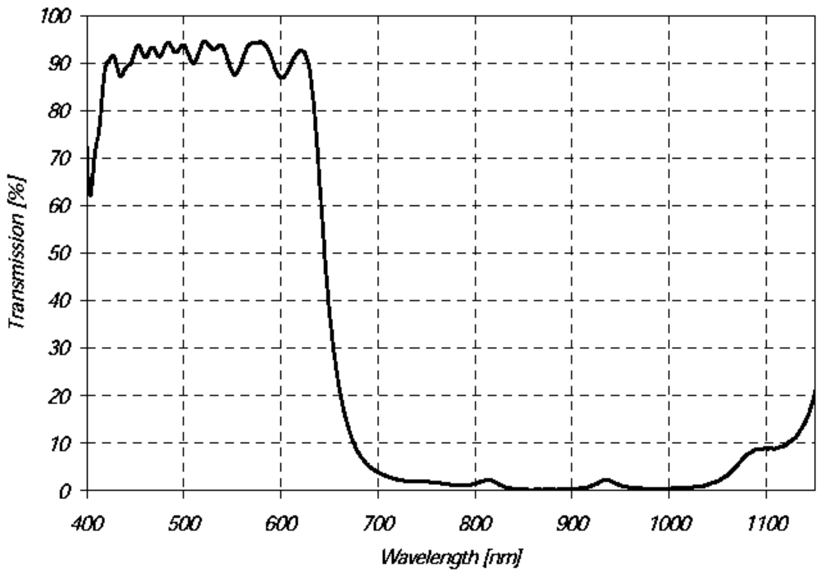


Figure 23: Approximate spectral transmission of IR cut filter (may vary slightly by filter lot) (type Jenofilt 217)

Focal length

Allied Vision offers different lenses from a variety of manufacturers. The following table lists selected image formats depending on camera type, distance and the focal length of the lens.

Note

All values listed in the following tables are theoretical and therefore only approximate values (focal length and field of view).

Pike F-032

Focal length	Field of view Distance = 0.5 m	Distance = 1 m
4.8 mm	0.38 m × 0.5 m	0.75 m × 1 m
8 mm	0.22 m × 0.29 m	0.44 m × 0.58 m
12 mm	0.15 m × 0.19 m	0.29 m × 0.38 m
16 mm	11 cm × 15 cm	22 cm × 29 cm
25 mm	6.9 cm × 9.2 cm	14 cm × 18 cm
35 mm	4.8 cm × 6.4 cm	9.6 cm × 13 cm
50 mm	3.3 cm × 4.4 cm	6.6 cm × 8.8 cm

Table 17: Pike F-032 focal length vs. field of view

Pike F-100, F-145, F-505

Focal length	Field of view Distance = 0.5 m	Distance = 1 m
4.8 mm	0.7 m × 0.9 m	1.4 m × 1.9 m
8 mm	0.4 m × 0.5 m	0.8 m × 1.1 m
12 mm	0.27 m × 0.36 m	0.54 m × 0.72 m
16 mm	0.2 m × 0.27 m	0.4 m × 0.54 m
25 mm	13 cm × 17 cm	26 cm × 34 cm
35 mm	8.8 cm × 12 cm	18 cm × 24 cm
50 mm	6 cm × 7.9 cm	12 cm × 17 cm

Table 18: Pike F-100, F-145, F-505 focal length vs. field of view

Pike F-210

Focal length	Field of view Distance = 0.5 m	Distance = 1 m
8 mm	0.6 m × 0.8 m	1.2 m × 1.6 m
12 mm	0.39 m × 0.52 m	0.78 m × 1.2 m
16 mm	0.29 m × 0.38 m	0.58 m × 0.76 m
25 mm	18 cm × 24 cm	36 cm × 49 cm
35 mm	13 cm × 17 cm	26 cm × 34 cm
50 mm	8.8 cm × 12 cm	18 cm × 23 cm

Table 19: Pike F-210 focal length vs. field of view

Note

Lenses with focal lengths < 35 mm will very likely show excessive shading in the edges of the image due to the fact that the image size of the sensor is slightly bigger than the C-mount itself and due to microlenses on the sensor's pixel.

Contact your Allied Vision distribution partner if you require non C-Mount lenses.

Pike F-421

Focal length	Field of view Distance = 0.5 m	Distance = 1 m
35 mm	20 cm × 20 cm	42 cm × 42 cm
50 mm	14 cm × 14 cm	29 cm × 29 cm

Table 20: Pike F-421 focal length vs. field of view

Pike F-1100, F-1600

	Field of view	
Focal length	**Distance = 0.5 m**	**Distance = 1 m**
18 mm	64 cm × 96 cm	1.3 m × 2.0 m
21 mm	55 cm × 82cm	1.1 m × 1.7 m
25 mm	46 cm × 68 cm	0.94 m × 1.4 m
28 mm	41 cm × 61 cm	0.83 m × 1.3 m
35 mm	32 cm × 48 cm	66 cm × 99 cm
50 mm	22 cm × 32 cm	46 cm × 68 cm
90 mm	11 cm × 16 cm	24 cm × 36 cm

Table 21: Pike F-1100, F-1600 focal length vs. field of view

Camera interfaces

This chapter gives you detailed information on status LEDs, inputs and outputs, trigger features and transmission of data packets.

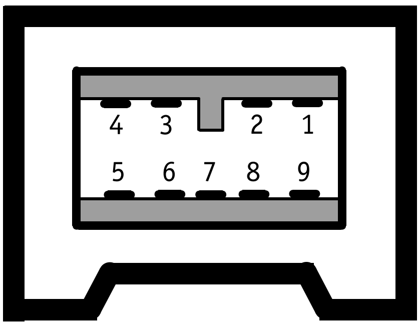
Note

For a detailed description of the camera interfaces (FireWire, I/O connector), ordering numbers and operating instructions see the *1394 Installation Manual*, Chapter *Camera interfaces*.

Read all notes and cautions in the *1394 Installation Manual*, before using any interfaces.

IEEE1394b port pin assignment

The IEEE1394b connector is designed for industrial use and has the following pin assignment as per specification:



Pin	Signal
1	TPB-
2	TPB+
3	TPA-
4	TPA+
5	TPA (Reference ground)
6	VG (GND)
7	N.C.
8	VP (Power, VCC)
9	TPB (Reference ground)

Figure 24: IEEE1394b connector

Note

- Both IEEE1394b screw-lock connectors connect to the IEEE1394 bus to control the camera and output frames. Connect the camera with connector. The other connector can be used to daisy chain a second camera.
- Cables with latching connectors on one or both sides can are available with l5 m or 7.5 m length. Contact your local distribution partner for more details.

www

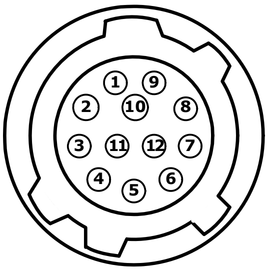
For more information on cables and on ordering cables online (by clicking the article and sending an inquiry) go to:

https://www.alliedvision.com/en/contact

Camera I/O connections

Caution

The camera is not intended to be connected to a DC distribution network. The maximum length for I/O cables must not exceed 30 m.



Pin	Signal	Direction	Level	Description	I/O cable color code
	Camera side Hirose HR25-7TR-12PA(73) connector				
1	External GND		GND for RS232 and ext. power	External Ground for RS232 and external power	Blue
2	External Power		+8 to +36 VDC	Power supply	Red
3	Camera Out 4	Out	Open emitter	Camera Output 4 (GPOut4) Default:-	Pink
4	Camera In 1	In	U_{in}*(high) = 3 V to U_{inVCC} U_{in}(low) = 0 V to 0.8 V	Camera Input 1 (GPIn1) Default: Trigger	Grey
5	Camera Out 3	Out	Open emitter	Camera Output 3 (GPOut3) Default: Busy	Yellow
6	Camera Out 1	Out	Open emitter	Camera Output 1 (GPOut1) Default: IntEna	Green
7	Camera In GND	In	Common GND for inputs	Camera Common Input Ground (In GND)	Brown
8	RxD RS232	In	RS232	Terminal Receive Data	White
9	TxD RS232	Out	RS232	Terminal Transmit Data	Black
10	Camera Out Power	In	Common VCC for outputs Max. 36 VDC	External Power for digital outputs (OutVCC)	Orange
11	Camera In 2	In	U_{in}*(high) = 3 V to U_{inVCC} U_{in}(low) = 0 V to 0.8 V	Camera Input 2 (GPIn2) Default:-	White/Black
12	Camera Out 2	Out	Open emitter	Camera Output 2 (GPOut2) Default: Follow CameraIn2	White/Brown
*min. 5 mA input current; U_{in} depends on input current					

Table 22: Camera I/O connector pin assignment and Pike I/O cable color coding

Note

12-pin Hirose I/O cables

The General Purpose I/O port uses a Hirose HR25-7TR-12PA(73) connector on the camera side. The mating cable connector is:

- Hirose HR25-7TP-12S(72) for soldering
- Hirose HR25-7TP-12SC(72) for crimping

Note

GP = General Purpose

For a detailed description of the I/O connector and its operating instructions see the *1394 Installation Manual*, Chapter *Pike input description*.

Read all Notes and Cautions in the *1394 Installation Manual*, before using the I/O connector.

Note

For cable color and pin out information, see the *Allied Vision I/O cable data sheet*:

https://www.alliedvision.com/en/support/technical-documentation/accessories-data-sheets.html

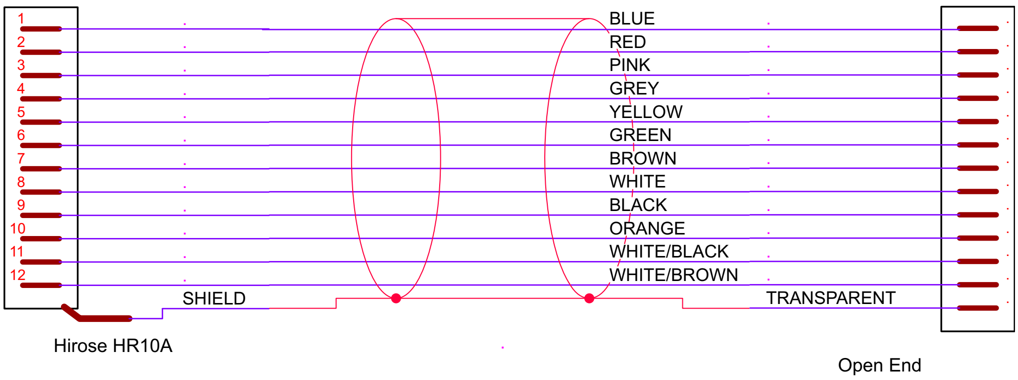


Figure 25: Pike cable color coding

Status LEDs

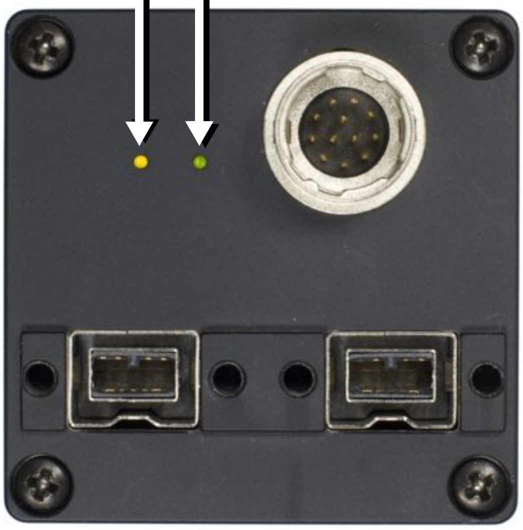


Figure 26: Position of status LEDs

On LED (green)

The green power LED indicates that the camera is being supplied with sufficient voltage and is ready for operation.

Status LED

The following states are displayed via the LED:

State	Description
Com/S1 (green)	Asynchronous and isochronous data transmission active (indicated asynchronously to transmission via the IEEE1394 bus)
Trg/S2 (yellow)	LED on- waiting for external trigger LED off- triggered / internal sync

Table 23: LED indication

Blink codes are used to signal warnings or error states:

Class S1 → / Error code S2 ↓	Warning 1 blink	DCAM 2 blinks	MISC 3 blinks	FPGA 4 blinks	Stack 5 blinks
FPGA boot error				1 to 5 blinks	
Stack setup					1 blink
Stack start					2 blinks
No FLASH object			1 blink		
No DCAM object		1 blink			
Register mapping		3 blinks			
VMode_ERROR_STATUS	1 blink				
FORMAT_7_ERROR_1	2 blinks				
FORMAT_7_ERROR_2	3 blinks				

Table 24: Error codes

The following sketch illustrates the series of blinks for a Format_7_error_1:

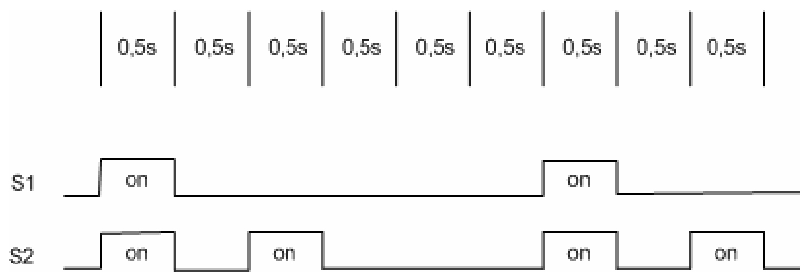


Figure 27: Warning and error states

You should wait for at least 2 full cycles because the display of blinking codes starts asynchronously - e.g. on the second blink from S2.

Control and video data signals

The inputs and outputs of the camera can be configured by software. The different modes are described below.

Inputs

Note

For a general description of the inputs and warnings see the *1394 Installation Manual*, Pike input description.

The optocoupler inverts all input signals. Inversion of the signal is controlled via the IO_INP_CTRL1..2 register (see Table 25: Advanced register: Input control on page 87).

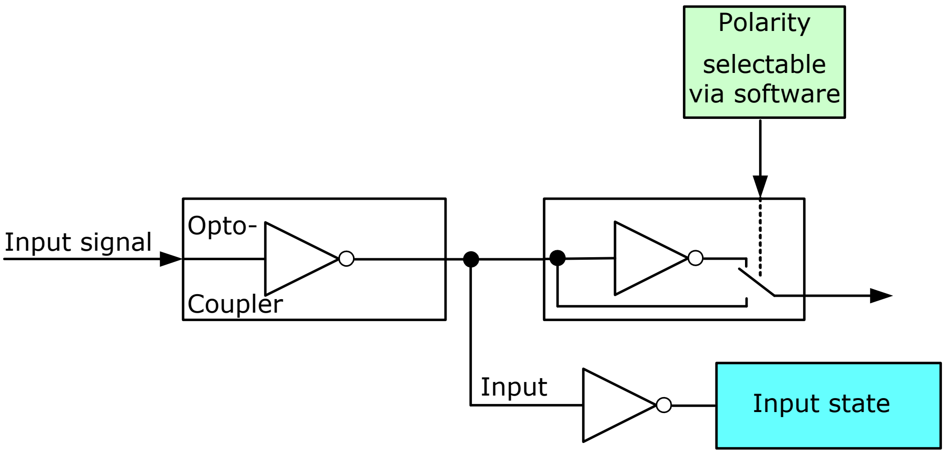


Figure 28: Input block diagram

Triggers

All inputs configured as triggers are linked by AND. If several inputs are being used as triggers, a high signal must be present on all inputs in order to generate a trigger signal. Each signal can be inverted. The camera must be set to external triggering to trigger image capture by the trigger signal.

Input/output pin control

All input and output signals running over the camera I/O connector are controlled by an advanced feature register.

Register	Name	Field	Bit	Description
0xF1000300	IO_INP_CTRL1	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 6]	Reserved
		Polarity	[7]	0: Signal not inverted 1: Signal inverted
		---	[8 to 10]	Reserved
		InputMode	[11 to 15]	Mode See Table 26: Input routing on page 87
		---	[16 to 30]	Reserved
		PinState	[31]	RD: Current state of pin
0xF1000304	IO_INP_CTRL2	Same as IO_INP_CTRL1		

Table 25: Advanced register: Input control

IO_INP_CTRL 1-2

The Polarity flag determines whether the input is low active (0) or high active (1). The input mode can be seen in the following table. The PinState flag is used to query the current status of the input.

The PinState bit reads the inverting optocoupler status after an internal negation. See Figure 28: Input block diagram on page 86.

This means that an open input sets the PinState bit to 0. (This is different to Allied Vision Marlin, where an open input sets PinState bit to 1.)

ID	Mode	Default
0x00	Off	
0x01	Reserved	
0x02	Trigger input	Input 1
0x03	Reserved	
0x06	Sequence Step	
0x07	Sequence Reset	
0x08 .. 0x1F	Reserved	

Table 26: Input routing

Note

If you set more than 1 input to function as a trigger input, all trigger inputs are ANDed.

Trigger delay

Pike cameras feature various ways to delay image capture based on external trigger.

With IIDC V1.31 there is a standard CSR at Register F0F00534/834h to control a delay up to FFFh × time base value.

The following table explains the inquiry register and the meaning of the various bits.

Register	Name	Field	Bit	Description
0xF0F00534	TRIGGER_DELAY_INQUIRY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Abs_Control_Inq	[1]	Capability of control with absolute value
		---	[2]	Reserved
		One_Push_Inq	[3]	One-push auto mode (controlled automatically by the camera once)
		Readout_Inq	[4]	Capability of reading out the value of this feature
		ON_OFF	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Auto mode (controlled automatically by the camera)
		Manual_Inq	[7]	Manual mode (controlled by user)
		Min_Value	[8 to 19]	Minimum value for this feature
		Max_Value	[20 to 31]	Maximum value for this feature

Table 27: Trigger delay inquiry register

Register	Name	Field	Bit	Description
0xF0F00834	TRIGGER_DELAY	Presence_Inq	[0]	Presence of this feature: 0:N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the value field 1: Control with value in the absolute value CSR. If this bit=1 the value in the value field has to be ignored.
		---	[2 to 5]	Reserved
		ON_OFF	[6]	Write ON or OFF this feature Read: Status of the feature ON=1 OFF=0
		---	[7 to 19]	Reserved
		Value	[20 to 31]	Value

Table 28: Trigger Delay CSR

The cameras also have an advanced register which allows even more precise image capture delay after receiving a hardware trigger.

Trigger delay advanced register

Register	Name	Field	Bit	Description
0xF1000400	TRIGGER_DELAY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	-
		ON_OFF	[6]	Trigger delay on/off
		---	[7 to 10]	-
		DelayTime	[11 to 31]	Delay time in µs

Table 29: Trigger delay advanced CSR

The advanced register allows the start of the integration to be delayed by max. 2^{21} µs, which is max. 2.1 s after a trigger edge was detected.

Note

- Switching trigger delay to ON also switches external Trigger_Mode_0 to ON.
- This feature works with external Trigger_Mode_0 only.

Outputs

Note

For a general description of the outputs and warnings see the *1394 Installation Manual*, Chapter Pike output description.

Output features are configured by software. Any signal can be placed on any output.

The main features of output signals are described below:

Signal	Description
IntEna (Integration Enable) signal	This signal displays the time in which exposure was made. By using a register this output can be delayed by up to 1.05 seconds.
Fval (Frame valid) signal	This feature signals readout from the sensor. This signal Fval follows IntEna.
Busy signal	This indicator appears when the exposure is being made; the sensor is being read from or data transmission is active. The camera is busy.

Table 30: Output signals

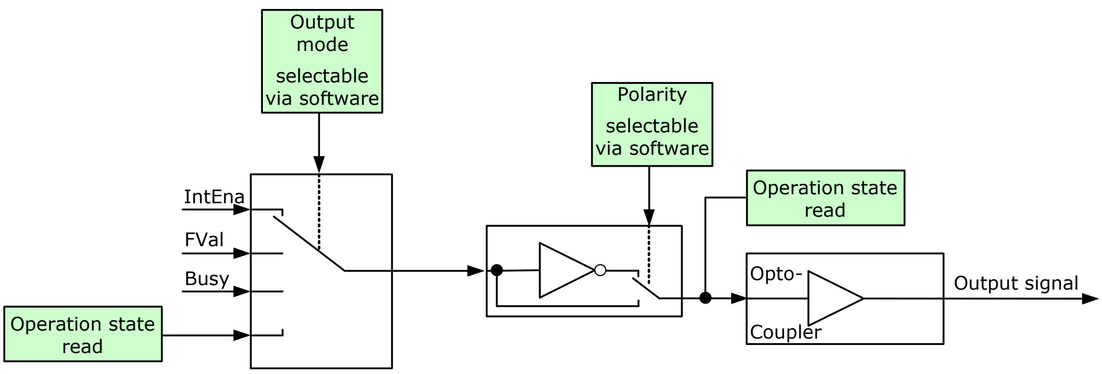


Figure 29: Output block diagram

IO_OUTP_CTRL 1-4

The outputs (Output mode, Polarity) are controlled via 4 advanced feature registers (see Table 31: Advanced register: Output control on page 91).

The Polarity field determines whether the output is inverted or not. The output mode can be viewed in the table below. The current status of the output can be queried and set via the PinState.

It is possible to read back the status of an output pin regardless of the output mode. This allows for example the host computer to determine if the camera is busy by simply polling the BUSY output.

Note

Outputs in Direct Mode:

For correct functionality the Polarity should always be set to 0 (SmartView: Trig/IO tab, Invert=No).

Register	Name	Field	Bit	Description
0xF1000320	IO_OUTP_CTRL1	Presence_Inq	[0]	Indicates presence of this feature (read only)
		PWMCapable	[1]	Indicates if an output pin supports the PWM feature. See Table 33: PWM configuration registers on page 94.
		---	[2 to 6]	Reserved
		Polarity	[7]	0: Signal not inverted 1: Signal inverted
		---	[8 to 10]	Reserved
		Output mode	[11 to 15]	Mode See Table 32: Output routing on page 92
		---	[16 to 30]	Reserved
		PinState	[31]	RD: Current state of pin WR: New state of pin
0xF1000324	IO_OUTP_CTRL2	Same as IO_OUTP_CTRL1		
0xF1000328	IO_OUTP_CTRL3	Same as IO_OUTP_CTRL1		
0xF100032C	IO_OUTP_CTRL4	Same as IO_OUTP_CTRL1		

Table 31: Advanced register: Output control

Output modes

ID	Mode	Default / description
0x00	Off	
0x01	Output state follows PinState bit	Using this mode, the Polarity bit has to be set to 0 (not inverted). This is necessary for an error free display of the output status.
0x02	Integration enable	Output 1
0x03	Reserved	
0x04	Reserved	
0x05	Reserved	
0x06	FrameValid	
0x07	Busy	Output 2
0x08	Follow corresponding input (Inp1→ Out1, Inp2 → Out2)	
0x09	PWM (=pulse-width modulation)	
0x0A..0x0F	Reserved	
0x10..0x1F	Reserved	

Table 32: Output routing

PinState 0 switches off the output transistor and produces a low level over the resistor connected from the output to ground.

The following diagram illustrates the dependencies of the various output signals.

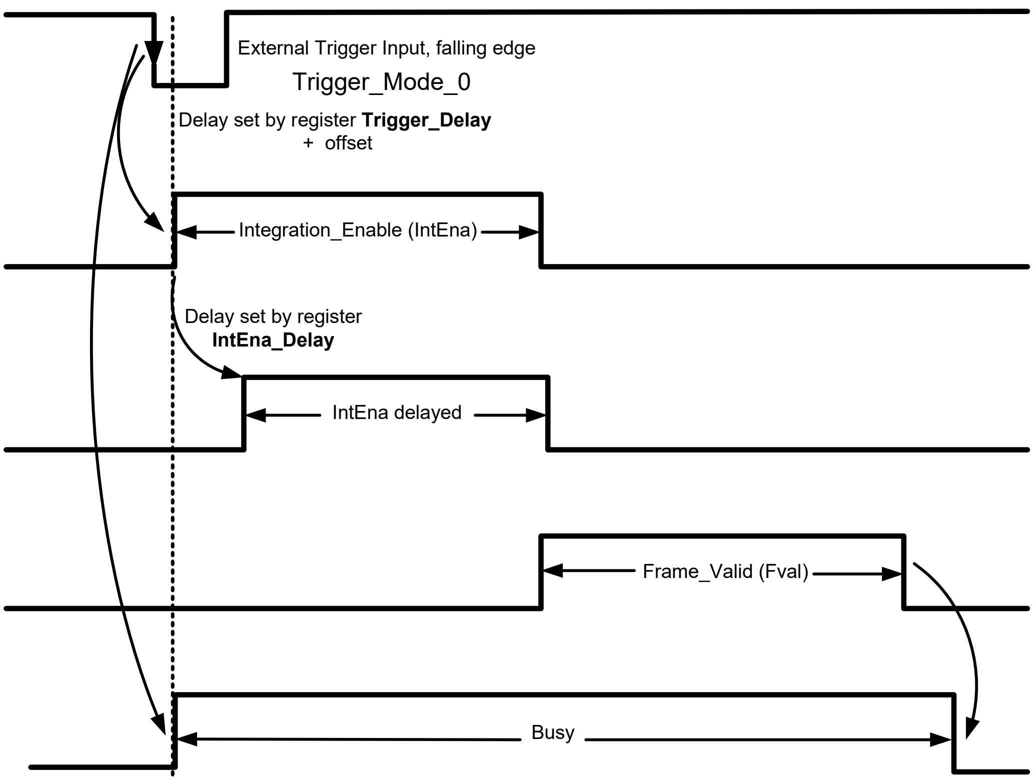


Figure 30: Output impulse diagram

Note

The signals can be inverted.

Caution

Firing a new trigger while IntEna is still active can result in missing image.

Note

- Note that trigger delay in fact delays the image capture whereas the IntEna_Delay only delays the leading edge of the IntEna output signal but does not delay the image capture.
- As mentioned before, it is possible to set the outputs by software. Doing so, the achievable maximum frequency is strongly dependent on individual software capabilities. As a rule of thumb, the camera itself will limit the toggle frequency to not more than 700 Hz.

Pulse-width modulation

The 2 inputs and 4 outputs are independent. Each output has pulse-width modulation (PWM) capabilities, which can be used (with additional external electronics) for motorized speed control or autofocus control.

Period (in µs) and pulse width (in µs) are adjustable via the following registers (see also examples in PWM: Examples in practice on page 95):

Register	Name	Field	Bit	Description
0xF1000800	IO_OUTP_PWM1	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1]	Reserved
		---	[2 to 3]	Reserved
		MinPeriod	[4 to 19]	Minimum PWM period in µs (read only)
		---	[20 to 27]	Reserved
		---	[28 to 31]	Reserved
0xF1000804		PulseWidth	[0 to 15]	PWM pulse width in µs
		Period	[16 to 31]	PWM period in µs
0xF1000808	IO_OUTP_PWM2	Same as IO_OUTP_PWM1		
0xF100080C				
0xF1000810	IO_OUTP_PWM3	Same as IO_OUTP_PWM1		
0xF1000814				
0xF1000818	IO_OUTP_PWM4	Same as IO_OUTP_PWM1		
0xF100081C				

Table 33: PWM configuration registers

To enable the PWM feature select output mode 0x09. Control the signal state via the PulseWidth and Period fields (all times in microseconds (µs)).

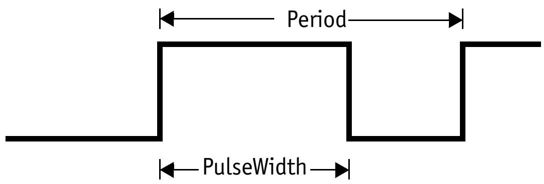


Figure 31: PulseWidth and Period definition

Note

Note the following conditions:

- PulseWidth < Period
- Period ≥ MinPeriod

PWM: minimum and maximum periods and frequencies

In the following formulas you find the minimum/maximum periods and frequencies for the pulse-width modulation (PWM).

$$\mathrm{period}_{min} = 3\mu s$$

$$\Rightarrow \mathrm{frequency}_{max} = \frac{1}{\mathrm{period}_{min}} = \frac{1}{3\mu s} = 333.33\mathrm{kHz}$$

$$\mathrm{frequency}_{min} = \frac{1}{2^{16} \times 10^{-6} s} = 15.26\mathrm{Hz}$$

$$\Rightarrow \mathrm{period}_{max} = \frac{1}{\mathrm{frequency}_{min}} = 2^{16}\mu s$$

Formula 1: Minimum/maximum period and frequency

PWM: Examples in practice

In this chapter we give you two examples, how to write values in the PWM registers. All values have to be written in microseconds (µs) in the PWM registers, therefore remember always the factor 10^{-6}s.

Example 1:

Set PWM with 1kHz at 30% pulse width.

$$\text{RegPeriod} = \frac{1}{\text{frequency} \times 10^{-6}\text{s}} = \frac{1}{1\,\text{kHz} \times 10^{-6}\text{s}} = 1000$$

$$\text{RegPulseWidth} = \text{RegPeriod} \times 30\% = 1000 \times 30\% = 300$$

Formula 2: PWM example 1

Example 2:

Set PWM with 250 Hz at 12% pulse width.

$$\text{RegPeriod} = \frac{1}{\text{frequency} \times 10^{-6}\text{s}} = \frac{1}{250\,\text{Hz} \times 10^{-6}\text{s}} = 4000$$

$$\text{RegPulseWidth} = \text{RegPeriod} \times 12\% = 4000 \times 12\% = 480$$

Formula 3: PWM example 2

Pixel data

Pixel data are transmitted as isochronous data packets in accordance with the IEEE1394 interface described in IIDC V1.31. The first packet of a frame is identified by the 1 in the sync bit (sy) of the packet header.

sync bit

<table>
<tr><th colspan="2">0 to 7</th><th colspan="2">8 to 15</th><th colspan="2">16 to 23</th><th colspan="2">24-31</th></tr>
<tr><td colspan="4">data_length</td><td>tg</td><td>channel</td><td>tCode</td><td>sy</td></tr>
<tr><td colspan="8">header_CRC</td></tr>
<tr><td colspan="8">Video data payload</td></tr>
<tr><td colspan="8">data_CRC</td></tr>
</table>

Table 34: Isochronous data block packet format. Source: IIDC V1.31

Field	Description
data_length	Number of bytes in the data field
tg	Tag field shall be set to zero
channel	Isochronous channel number, as programmed in the iso_channel field of the cam_sta_ctrl register
tCode	Transaction code shall be set to the isochronous data block packet tCode
sy	Synchronization value (sync bit) This is one single bit. It indicates the start of a new frame. It shall be set to 0001h on the first isochronous data block of a frame, and shall be set to zero on all other isochronous blocks
Video data payload	Shall contain the digital video information

Table 35: Description of data block packet format

- The video data for each pixel are output in either 8-bit or 14-bit format (Packed 12-Bit Mode: 12-bit format).
- Each pixel has a range of 256 or 16384 (Packed 12-Bit Mode: 4096) shades of gray.
- The digital value 0 is black and 255 or 16383 (Packed 12-Bit Mode: 4095) is white. In 16-bit mode the data output is MSB aligned.

Description of video data formats

The following tables provide a description of the video data format for the different modes. (Source: IIDC V1.31; packed 12-bit mode: Allied Vision)

<YUV8 (4:2:2) format>

Each component has 8-bit data.

<YUV8 (4:2:2) format>			
$U_{(K+0)}$	$Y_{(K+0)}$	$V_{(K+0)}$	$Y_{(K+1)}$
$U_{(K+2)}$	$Y_{(K+2)}$	$V_{(K+2)}$	$Y_{(K+3)}$
$U_{(K+4)}$	$Y_{(K+4)}$	$V_{(K+4)}$	$Y_{(K+5)}$
$U_{(K+Pn-6)}$	$Y_{(K+Pn-6)}$	$V_{(K+Pn-6)}$	$Y_{(K+Pn-5)}$

Table 36: YUV8 (4:2:2) format: Source: IIDC V1.31

<YUV8 (4:2:2) format>			
$U_{(K+Pn-4)}$	$Y_{(K+Pn-4)}$	$V_{(K+Pn-4)}$	$Y_{(K+Pn-3)}$
$U_{(K+Pn-2)}$	$Y_{(K+Pn-2)}$	$V_{(K+Pn-2)}$	$Y_{(K+Pn-1)}$

Table 36: YUV8 (4:2:2) format: Source: IIDC V1.31 (continued)

<YUV8 (4:1:1 format)

Each component has 8-bit data.

<YUV8 (4:1:1) format>			
$U_{(K+0)}$	$Y_{(K+0)}$	$Y_{(K+1)}$	$V_{(K+0)}$
$Y_{(K+2)}$	$Y_{(K+3)}$	$U_{(K+4)}$	$Y_{(K+4)}$
$Y_{(K+5)}$	$V_{(K+4)}$	$Y_{(K+6)}$	$Y_{(K+7)}$
$U_{(K+Pn-8)}$	$Y_{(K+Pn-8)}$	$Y_{(K+Pn-7)}$	$V_{(K+Pn-8)}$
$Y_{(K+Pn-6)}$	$Y_{(K+Pn-5)}$	$U_{(K+Pn-4)}$	$Y_{(K+Pn-4)}$
$Y_{(K+Pn-3)}$	$V_{(K+Pn-4)}$	$Y_{(K+Pn-2)}$	$Y_{(K+Pn-1)}$

Table 37: YUV8 (4:1:1) format: Source: IIDC V1.31

<Y (Mono8/Raw8) format>

Y component has 8-bit data.

<Y (Mono8/Raw8) format>			
$Y_{(K+0)}$	$Y_{(K+1)}$	$Y_{(K+2)}$	$Y_{(K+3)}$
$Y_{(K+4)}$	$Y_{(K+5)}$	$Y_{(K+6)}$	$Y_{(K+7)}$
$Y_{(K+Pn-8)}$	$Y_{(K+Pn-7)}$	$Y_{(K+Pn-6)}$	$Y_{(K+Pn-5)}$
$Y_{(K+Pn-4)}$	$Y_{(K+Pn-3)}$	$Y_{(K+Pn-2)}$	$Y_{(K+Pn-1)}$

Table 38: Y (Mono8) format: Source: IIDC V1.31 / Y (Raw8) format: Allied Vision

<Y (Mono16/Raw16) format>

Y component has 16-bit data.

<Y (Mono16) format>	
High byte	Low byte
$Y_{(K+0)}$	$Y_{(K+1)}$
$Y_{(K+2)}$	$Y_{(K+3)}$
$Y_{(K+Pn-4)}$	$Y_{(K+Pn-3)}$
$Y_{(K+Pn-2)}$	$Y_{(K+Pn-1)}$

Table 39: Y (Mono16) format: Source: IIDC V1.31

<Y (Mono12/Raw12) format>

<Y (Mono12) format>			
$Y_{(K+0)}$ [11..4]	$Y_{(K+1)}$ [3..0] $Y_{(K+0)}$ [3..0]	$Y_{(K+1)}$ [11..4]	$Y_{(K+2)}$ [11..4]
$Y_{(K+3)}$ [3..0] $Y_{(K+2)}$ [3..0]	$Y_{(K+3)}$ [11..4]	$Y_{(K+4)}$ [11..4]	$Y_{(K+5)}$ [3..0] $Y_{(K+4)}$ [3..0]
$Y_{(K+5)}$ [11..4]	$Y_{(K+6)}$ [11..4]	$Y_{(K+7)}$ [3..0] $Y_{(K+6)}$ [3..0]	$Y_{(K+7)}$ [11..4]

Table 40: Packed 12-Bit Mode (mono and raw) Y12 format (Allied Vision)

<Y(Mono8/Raw8), RGB8>

Each component (Y, R, G, B) has 8-bit data. The data type is *Unsigned Char*.

Y, R, G, B	Signal level (decimal)	Data (hexadecimal)
Highest	255	0xFF
	254	0xFE
	.	.
	.	.
	1	0x01
Lowest	0	0x00

Figure 32: Data structure of Mono8, RGB8; Source: IIDC V1.31 / Y(Mono8/Raw8) format: Allied Vision

<YUV8>

Each component (Y, U, V) has 8-bit data. The Y component is the same as in the above table.

U, V	Signal level (decimal)	Data (hexadecimal)
Highest (+)	127	0xFF
	126	0xFE
	.	.
	.	.
	1	0x81
Lowest	0	0x80
	-1	0x7F
	-127	0x01
Highest (-)	-128	0x00

Figure 33: Data structure of YUV8; Source: IIDC V1.31

<Y(Mono16)>

Y component has 16-bit data. The data type is *Unsigned Short (big-endian)*.

Y	Signal level (decimal)	Data (hexadecimal)
Highest	65535	0xFFFF
	65534	0xFFFE
	.	.
	.	.
	1	0x0001
Lowest	0	0x0000

Figure 34: Data structure of Y(Mono16); Source: IIDC V1.31

<Y(Mono12)>

Y component has 12-bit data. The data type is *unsigned*.

Y	Signal level (decimal)	Data (hexadecimal)
Highest	4095	0x0FFF
	4094	0x0FFE
	.	.
	.	.
	1	0x0001
Lowest	0	0x0000

Table 41: Data structure of Packed 12-Bit Mode (mono and raw) (Allied Vision)

Description of the data path

Pike block diagrams

The following diagrams illustrate the data flow and the bit resolution of image data after being read from the CCD sensor chip in the camera. The individual blocks are described in more detail in the following paragraphs. For sensor data see Specifications on page 45.

Monochrome models

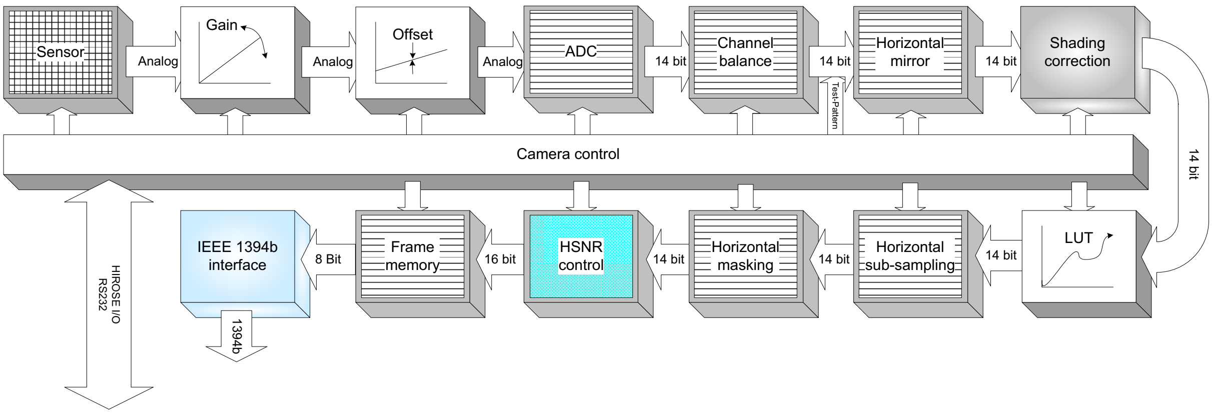


Figure 35: Block diagram: monochrome models

Color models

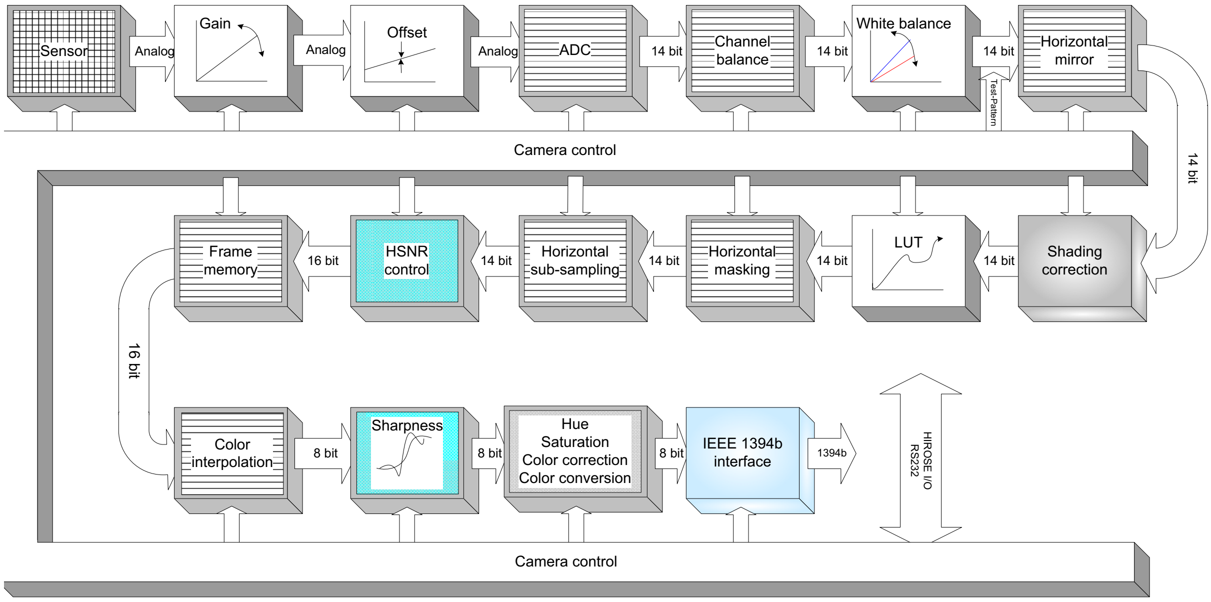


Figure 36: Block diagram: color models

Channel balance

All ON Semiconductor Pike sensors and the Sony Semiconductor sensor (of Pike F-505) are read out via two channels: the first channel for the left half of the image and the second channel for the right half of the image (divided by a central vertical line).

Note

Pike F-1100 and Pike F-1600 can also be used in single-tap readout mode, to prevent channel balance related problems.

See Sensor digitization taps (Pike F-1100, F-1600 only) on page 321ff.

All ON Semiconductor equipped cameras come with a sensor-specific pre-adjusted channel balance.

However in some cases it may be advantageous to carry out a fine adjustment with the so-called channel balance.

To carry out a gain adjustment in an advanced register, see Table 175: Advanced register: Channel balance on page 313.

To carry out a dual-tap offset adjustment in an advanced register, see Table 176: Advanced register: Dual-tap offset adjustment on page 313

Note

Automatic adjustment of gain (and offset) is implemented in SmartView and is not available on register basis.

Channel adjustment with SmartView (>1.5)

Prerequisites:

- Test sheet with continuous monochrome gradient
- Pike camera with defocused lens
- Pike color cameras set to RAW8 or RAW16 (debayering: none)
- In case of using AOI, be aware that the middle vertical line (+/- 20 pixel) is part of the AOI.

To carry out an adjustment in SmartView, perform the following steps:

1. In SmartView click **Extras → Adjust channels...** or use **Alt+Ctrl+A**.

   The following window opens:

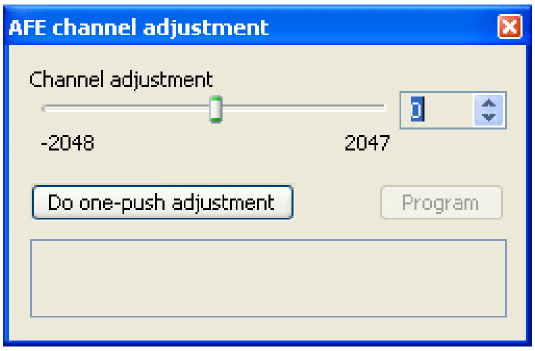


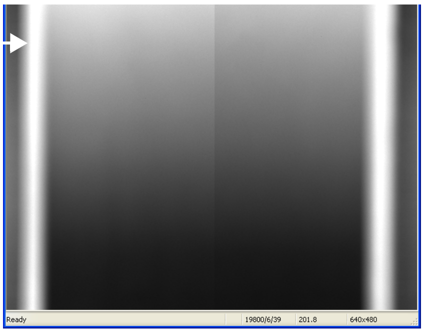
Figure 37: SmartView: channel adjustment (>1.5 up to 1.9.1)

Note

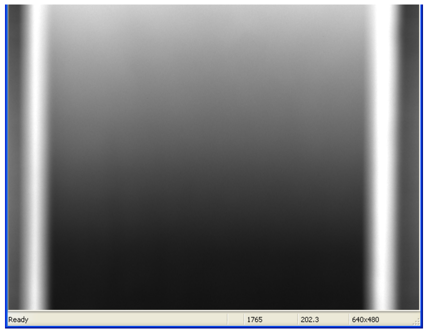
Program button is only available for Allied Vision.

2. To perform an automatic channel adjustment, click on **Do one-push adjustment**.
3. If the adjustment is not sufficient, repeat this step or adjust by clicking the arrow buttons.

The two channels are automatically adjusted. For the channel adjustment a region from +/- 20 pixel around the middle vertical is taken into account.



before



after

Figure 38: Example of channel adjustment: Pike F-032B

Dual-tap offset adjustment with SmartView (1.10 or greater)

Prerequisites:

- Lens cap
- Test sheet with continuous monochrome gradient
- Only following cameras: Pike F-032, Pike F-100, Pike F-210, Pike F-421, Pike F-505, Pike F-1100, and Pike F-1600
- Pike camera with defocused lens
- Pike color cameras set to RAW8 or RAW16 (debayering: none)
- In case of using AOI, be aware that the middle vertical line (+/- 20 pixel) is part of the AOI.
- First do offset adjustment, then do gain adjustment.

To carry out an adjustment (offset adjustment + gain adjustment) in SmartView, perform the following steps:

1. In SmartView click **Extras** → **Adjust channels...** or use **Alt+Ctrl+A**.

   The following window opens:

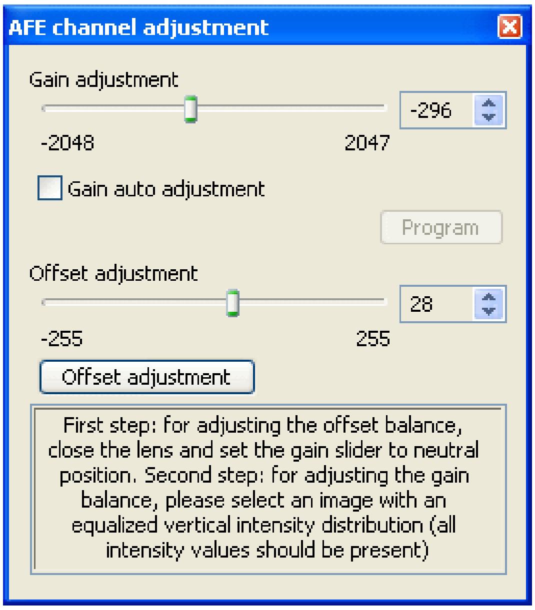


Figure 39: SmartView: channel adjustment (gain+offset) (1.10 and greater)

2. Put on lens cap.
3. Set gain adjustment slider and offset adjustment slider to 0.
4. Click several times **Offset adjustment** until the slider does not move any more.
5. Put off lens cap.
6. Take test sheet with vertical continuous monochrome gradient, defocus lens and start image acquisition.
7. Activate **Gain auto adjustment**.

   Now left and right channel should be adjusted for all gray values, so that vertical line is no more visible.
8. To save these settings in the user profiles, see User profiles on page 330ff. and Table 197: User profile: stored settings on page 333 (CHANNEL_ADJUST_CTRL, CHANNEL_ADJUST_VALUE, ADV_CHN_ADJ_OFFSET, ADV_CHN_ADJ_OFFSET+1).

Note

Channel adjustment should be done in the same gain region as in your real application.

If you use a much greater gain in your application, it may be necessary to do the dual-tap offset adjustment again.

Dual-tap offset adjustment is done once in the Allied Vision factory and saved via **Program** button in User set 0.

The **Program** button is not available for the user.

White balance

There are two types of white balance:

- one-push white balance: white balance is done only once (not continuously)
- auto white balance (AWB): continuously optimizes the color characteristics of the image

Pike color cameras have both one-push white balance and auto white balance. White balance is applied so that non-colored image parts are displayed non-colored.

From the user's point, the white balance settings are made in register 80Ch of IIDC V1.31. This register is described in more detail below.

Register	Name	Field	Bit	Description
0xF0F0080C	WHITE_BALANCE	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the **Value** field 1: Control with value in the **Absolute** value CSR If this bit=1, the value in the **Value** field will be ignored.
		---	[2 to 4]	Reserved
		One_Push	[5]	Write 1: begin to work (self-cleared after operation) Read: 1: in operation 0: not in operation If A_M_Mode = 1, this bit will be ignored.
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON
		A_M_MODE	[7]	Write: set mode Read: read current mode 0: MANUAL 1: AUTO
		U/B_Value	[8 to 19]	U/B value This field is ignored when writing the value in Auto or OFF mode. If readout capability is not available, reading this field has no meaning.
		V/R_Value	[20 to 31]	V/R Value This field is ignored when writing the value in Auto or OFF mode. If readout capability is not available, reading this field has no meaning.

Table 42: White balance register

The values in the **U/B_Value** field produce changes from green to blue; the **V/R_Value** field from green to red as illustrated below.

Note

While lowering both U/B and V/R registers from 284 towards 0, the lower one of the two effectively controls the green gain.

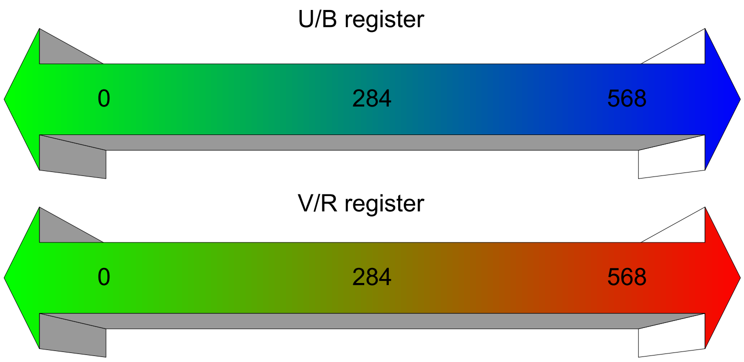


Figure 40: U/V slider range

Type	Range	Range in dB
Pike color cameras	0 to 568	± 10 dB

Table 43: Manual range of U/B and V/R for Pike models

The increment length is ~0.0353 dB/step.

One-push white balance

Note

Configuration

To configure this feature in control and status register (CSR), see Table 42: White balance register on page 108.

The camera automatically generates frames, based on the current settings of all registers (GAIN, OFFSET, SHUTTER, etc.).

For white balance, in total **9** frames are processed. For the white balance algorithm the whole image or a subset of it is used. The R-G-B component values of the samples are added and are used as actual values for the one-push white balance.

This feature uses the assumption that the R-G-B component sums of the samples shall be equal; i.e., it assumes that the average of the sampled grid pixels is to be monochrome.

Note

The following ancillary conditions should be observed for successful white balance:

- There are no stringent or special requirements on the image content, it requires only the presence of equally weighted RGB pixels in the image.

If the image capture is active (e.g. **IsoEnable** set in register 614h), the frames used by the camera for white balance are also output on the IEEE1394 bus. Any previously active image capture is restarted after the completion of white balance.

The following flow diagram illustrates the one-push white balance sequence.

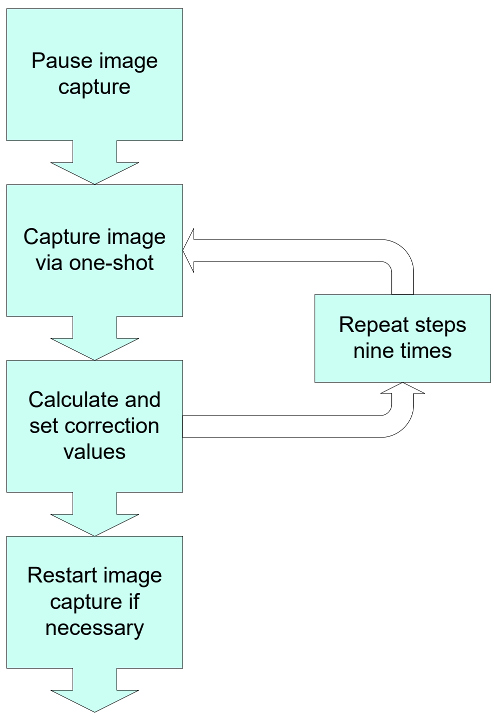


Figure 41: One-push white balance *sequence*

Finally, the calculated correction values can be read from the WHITE_BALANCE register 80Ch.

Auto white balance (AWB)

There is also an auto white balance feature available which continuously optimizes the color characteristics of the image.

For the white balance algorithm the whole image or a subset of it is used.

Auto white balance can also be enabled by using an external trigger. However, if there is a pause of >10 seconds between capturing individual frames this process is aborted.

Note

The following ancillary conditions should be observed for successful white balance:

- There are no stringent or special requirements on the image content, it requires only the presence of equally weighted RGB pixels in the image.
- Automatic white balance can be started both during active image capture and when the camera is in idle state.

Note

Configuration

To set position and size of the control area (Auto_Function_AOI) in an advanced register, see Table 171: Advanced register: Autofunction AOI on page 310.

AUTOFNC_AOI affects the auto shutter, auto gain and auto white balance features and is independent of the Format7 AOI settings. If this feature is switched off the work area position and size will follow the current active image size.

Within this area, the R-G-B component values of the samples are added and used as actual values for the feedback.

The following drawing illustrates the AUTOFNC_AOI settings in greater detail.

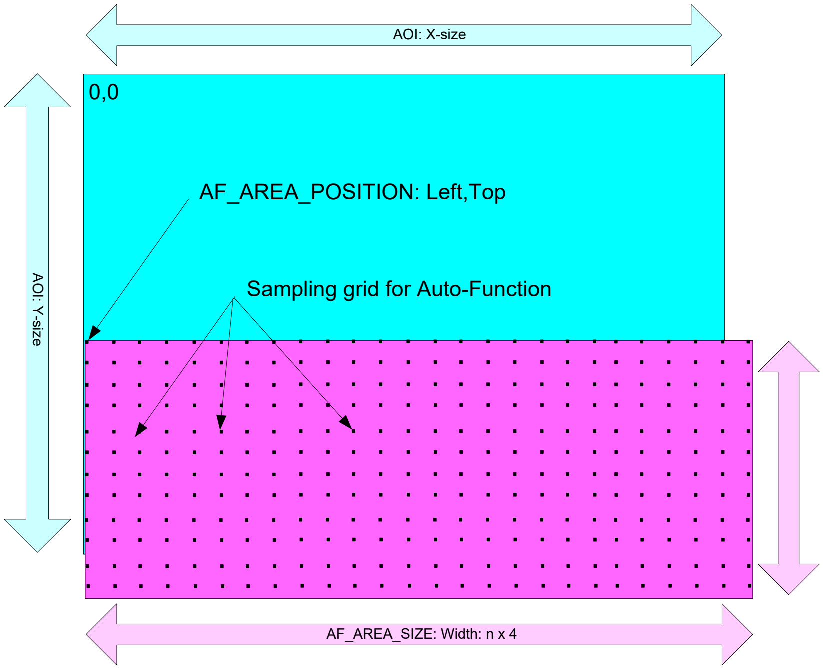


Figure 42: AUTOFNC_AOI positioning

The algorithm is based on the assumption that the R-G-B component sums of the samples are equal, i.e., it assumes that the mean of the sampled grid pixels is to be monochrome.

Auto shutter

In combination with auto white balance, Pike cameras are equipped with auto-shutter feature.

When enabled, the auto shutter adjusts the shutter within the default shutter limits or within those set in advanced register F1000360h in order to reach the reference brightness set in auto exposure register.

Note

Target gray level parameter in SmartView corresponds to Auto_exposure register 0xF0F00804 (IIDC).

Increasing the auto exposure value increases the average brightness in the image and vice versa.

Increasing the auto exposure value increases the average brightness in the image and vice versa.

The applied algorithm uses a proportional plus integral controller (PI controller) to achieve minimum delay with zero overshot.

To configure this feature in control and status register (CSR):

Register	Name	Field	Bit	Description
0xF0F0081C	SHUTTER	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the **Value** field 1: Control with value in the **Absolute** value CSR If this bit=1, the value in the **Value** field will be ignored.
		---	[2 to 4]	Reserved
		One_Push	[5]	Write 1: begin to work (self-cleared after operation) Read: 1: in operation 0: not in operation If A_M_Mode = 1, this bit will be ignored.
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON
		A_M_MODE	[7]	Write: set mode Read: read current mode 0: MANUAL 1: AUTO
		---	[8 to 19]	Reserved
		Value	[20 to 31]	Read/Write Value This field is ignored when writing the value in Auto or OFF mode. If readout capability is not available, reading this field has no meaning.

Table 44: CSR: Shutter

Note

Configuration

To configure this feature in an advanced register, see Table 169: Advanced register: Auto shutter control on page 307.

Auto gain

All Pike cameras are equipped with auto gain feature.

Note

Configuration

To configure this feature in an advanced register, see Table 170: Advanced register: Auto gain control on page 309.

When enabled auto gain adjusts the gain within the default gain limits or within the limits set in advanced register F1000370h in order to reach the brightness set in auto exposure register as reference.

Increasing the auto exposure value (aka **target gray value**) increases the average brightness in the image and vice versa.

The applied algorithm uses a proportional plus integral controller (PI controller) to achieve minimum delay with zero overshot.

The following table shows both the gain and auto exposure CSR.

Register	Name	Field	Bit	Description
0xF0F00820	GAIN	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the value field 1: Control with value in the absolute value CSR If this bit=1 the value in the value field has to be ignored.
		---	[2 to 4]	Reserved
		One_Push	[5]	Write: Set bit high to start Read: Status of the feature: Bit high: WIP Bit low: Ready
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON
		A_M_MODE	[7]	Write: set mode Read: read current mode 0: MANUAL 1: AUTO
		---	[8 to 19]	Reserved
		Value	[20 to 31]	Read/Write Value This field is ignored when writing the value in Auto or OFF mode. If readout capability is not available, reading this field has no meaning.

Table 45: CSR: Gain

Register	Name	Field	Bit	Description
0xF0F00804	AUTO_EXPOSURE	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the value field 1: Control with value in the absolute value CSR If this bit=1 the value in the value field has to be ignored.
		---	[2 to 4]	Reserved
		One_Push	[5]	Write: Set bit high to star Read: Status of the feature: Bit high: WIP Bit low: Ready
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON
		A_M_MODE	[7]	Write: set mode Read: read current mode 0: MANUAL 1: AUTO
		---	[8 to 19]	Reserved
		Value	[20 to 31]	Read/Write Value This field is ignored when writing the value in Auto or OFF mode. If readout capability is not available, reading this field has no meaning.

Table 46: CSR: Auto Exposure

Note

To configure auto gain control in an advanced register, see Table 170: Advanced register: Auto gain control on page 309.

Note

- Values can only be changed within the limits of gain CSR.
- Changes in auto exposure register only have an effect when auto gain is active.
- Auto exposure limits are 50 to 205. (**SmartView→Ctrl1 tab**: **Target gray level**)

Manual gain

Pike cameras are equipped with a gain setting, allowing the gain to be manually adjusted on the fly by means of a simple command register write.

The following ranges can be used when manually setting the gain for the analog video signal:

Type	Range	Range in dB	Increment length
Pike color models	0 to 565	0 to 20 dB	~0.0353 dB/step
Pike monochrome models	1 to 630	0 to 22 dB	
Pike F-145B	0 to 900	0 to 32 dB	~0.0358 dB/step
Pike F-145C	0 to 900	0 to 32 dB	
Pike F-145B-15fps	0 to 900	0 to 32 dB	~0.0358 dB/step
Pike F-145C-15fps	0 to 900	0 to 32 dB	
Pike F-505B	0 to 670	0 to 24 dB	~0.0359 dB/step
Pike F-505C	0 to 670	0 to 24 dB	
Pike F-1100B	0 to 670	0 to 24 dB	~0.0359 dB/step
Pike F-1100C	0 to 670	0 to 24 dB	
Pike F-1600B	0 to 670	0 to 24 dB	~0.0359 dB/step
Pike F-1600C	0 to 670	0 to 24 dB	

Table 47: Manual gain range for Pike models

Note

- Setting the gain does not change the offset (black value)
- A higher gain produces greater image noise. This reduces image quality. For this reason, try first to increase the brightness, using the aperture of the camera optics and/or longer shutter settings.

Brightness (black level or offset)

It is possible to set the black level in the camera within the following ranges:

0 to +16 gray values (@ 8 bit)

Increments @ 8 bit for Pike cameras:

Pike model	Increments [LSB]
F-032B, F-032C	1/16
F-100B, F-100C	1/16
F-145B, F-145C	1/64
F-210B	1/16
F-421B, F-421C	1/16
F-505B, F-505C	1/64
F-1100B, F-1100C	1/64

Table 48: Increments for setting the black level

Note Setting the gain does not change the offset (black value).

The IIDC register brightness at offset 800h is used for this purpose.

The following table shows the BRIGHTNESS register.

Register	Name	Field	Bit	Description
0xF0F00800	BRIGHTNESS	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the value field 1: Control with value in the absolute value CSR If this bit= 1 the value in the value field has to be ignored
		---	[2 to 4]	Reserved
		One_Push	[5]	Write: Set bit high to start Read: Status of the feature: Bit high: WIP Bit low: Ready
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON
		A_M_MODE	[7]	Write: set mode Read: read current mode 0: MANUAL 1: AUTO
		---	[8 to 19]	Reserved
		Value	[20 to 31]	Read/Write Value; this field is ignored when writing the value in Auto or OFF mode; if readout capability is not available reading this field has no meaning

Table 49: CSR: Brightness

Horizontal mirror function

All Pike cameras are equipped with an electronic mirror function, which mirrors pixels from the left side of the image to the right side and vice versa. The mirror is centered to the actual **FOV** center and can be combined with all image manipulation functions, like **binning** and **shading**.

This function is especially useful when the camera is looking at objects with the help of a mirror or in certain microscopy applications.

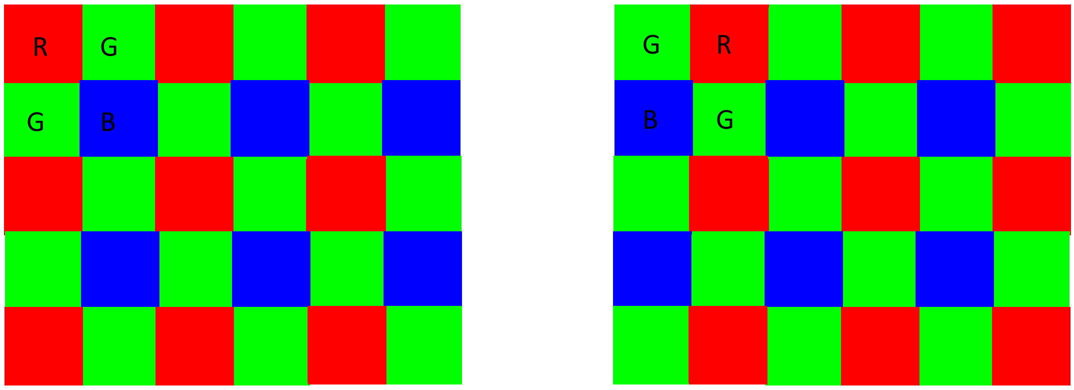
Note

Configuration

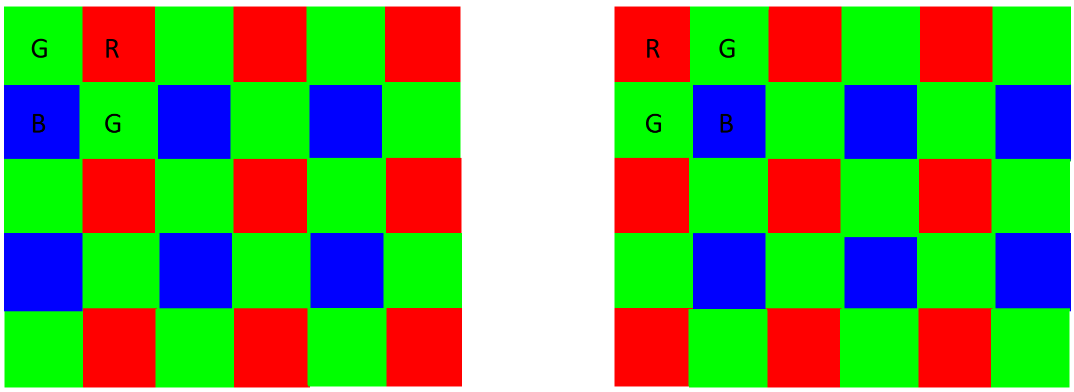
To configure this feature in an advanced register, see Table 174: Advanced register: Mirror image on page 312.

Note

The use of the mirror function with color cameras and image output in RAW format has implications on the Bayer-ordering of the colors.



Mirror OFF: R-G-G-B for Pike F-145C and F-505C Mirror ON: G-R-B-G Pike 145 C and Pike F-505C



Mirror OFF: G-R-B-G for all other Pike models Mirror ON: R-G-G-B for all other Pike models

Figure 43: Mirror and Bayer order

Note

During switchover one image may be temporarily corrupted.

Shading correction

Shading correction is used to compensate for non-homogeneities caused by lighting or optical characteristics within specified ranges.

To correct a frame, a multiplier from 1 to 2 is calculated for each pixel in 1/256 steps: this allows for shading to be compensated by up to 50%.

Besides generating shading data off-line and downloading it to the camera, the camera allows correction data to be generated automatically in the camera itself.

Note

- Shading correction does not support the mirror function.
- If you use shading correction, do not change the mirror function.
- Due to binning and sub-sampling in the Format_7 modes read the following hints to build shading image in Format_7 modes.

Building shading image in Format_7 modes

horizontal — Binning/sub-sampling is always done after shading correction. Shading is always done on full horizontal resolution. Therefore shading image has always to be built in full horizontal resolution.

vertical — Binning/sub-sampling is done in the sensor, before shading correction. Therefore shading image has to be built in the correct vertical resolution.

Note

Build shading image always with the full horizontal resolution (0 × horizontal binning / 0 × horizontal sub-sampling), but with the desired vertical binning/sub-sampling.

First example

4 × horizontal binning, 2 × vertical binning
⇨ build shading image with 0 × horizontal binning and 2 × vertical binning

Second example

2 out of 16 horizontal sub-sampling, 2 out of 8 vertical sub-sampling
⇨ build shading image with 0 × horizontal binning and 2 out of 8 vertical sub-sampling

How to store shading image

There are two storing possibilities:

- After generating the shading image in the camera, it can be uploaded to the host computer for nonvolatile storage purposes.
- The shading image can be stored in the camera itself.

The following pictures describe the process of automatic generation of correction data (Pike F-032C). Surface plots and histograms were created using the **ImageJ** program.

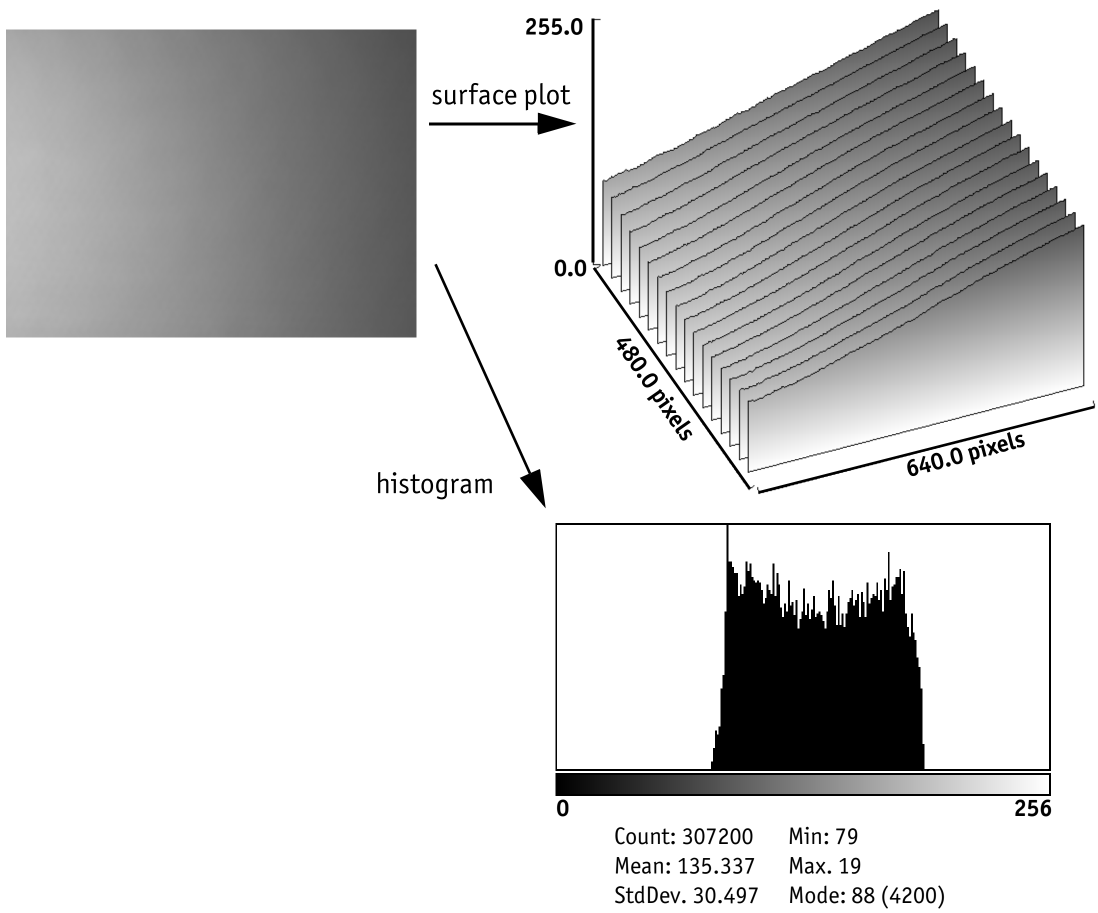


Figure 44: Shading correction: Source image with non-uniform illumination

- On the left you see the source image with non-uniform illumination.
- The surface plot on the right clearly shows a gradient of the brightness (0: brightest → 255: darkest pixels).
- The histogram shows a wide band of gray values.

By defocusing the lens, high-frequency image data is removed from the source image, therefore its not included in the shading image.

Automatic generation of correction data

Requirements

Shading correction compensates for non-homogeneities by giving all pixels the same gray value as the brightest pixel. This means that only the background must be visible and the brightest pixel has a gray value of less than 255 when automatic generation of shading data is started.

It may be necessary to use a neutral white reference, e.g. a piece of paper, instead of the real image.

Algorithm

After the start of automatic generation, the camera pulls in the number of frames set in the GRAB_COUNT register. Recommended values are 2, 4, 8, 16, 32, 64, 128 or 256. An arithmetic mean value is calculated from them (to reduce noise).

After this, a search is made for the brightest pixel in the mean value frame. The brightest pixel(s) remain unchanged. A factor is then calculated for each pixel to be multiplied by, giving it the gray value of the brightest pixel.

All of these multipliers are saved in a shading reference image. The time required for this process depends on the number of frames to be calculated and on the resolution of the image.

Correction alone can compensate for shading by up to 50% and relies on full resolution data to minimize the generation of missing codes.

How to proceed:

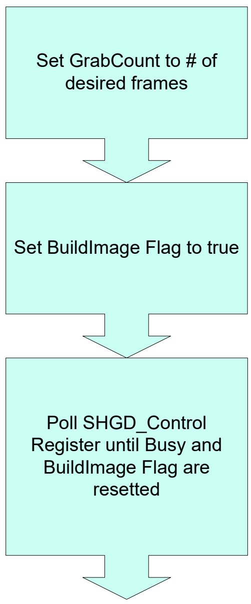


Figure 45: Automatic generation of a shading image

Note

Configuration and storing non-volatile

To configure this feature in an advanced register, see Table 164: Advanced register: Shading on page 302.

To store shading image data into **non-volatile memory**, see Non-volatile memory operations on page 304.

Note

- The SHDG_CTRL register should not be queried at very short intervals. This is because each query delays the generation of the shading image. An optimal interval time is 500 ms.

Note

- The calculation of shading data is always carried out at the current resolution setting. If the AOI is later larger than the window in which correction data was calculated, none of the pixels lying outside are corrected.
- For Format_7 mode, it is advisable to generate the shading image in the largest displayable frame format. This ensures that any smaller AOIs are completely covered by the shading correction.
- The automatic generation of shading data can also be enabled when image capture is already running. The camera then pauses the running image capture for the time needed for generation and resumes after generation is completed.
- Shading correction can be combined with the image mirror and gamma functionality.
- Changing binning modes involves the generation of new shading reference images due to a change in the image size.

After the lens has been focused again the image below will be seen, but now with a considerably more uniform gradient.

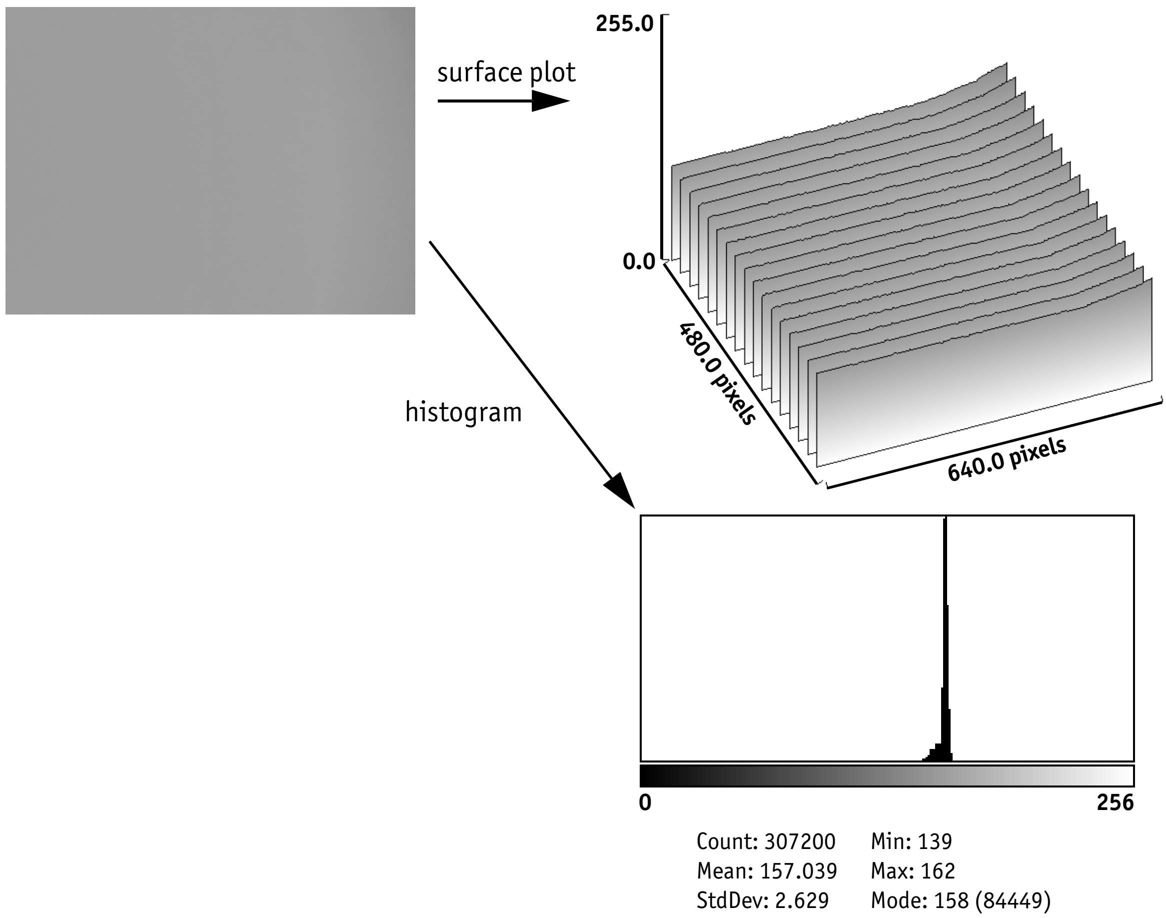


Figure 46: Example of shaded image

- On the left you see the image after shading correction.
- The surface plot on the right clearly shows nearly no more gradient of the brightness (0: brightest → 255: darkest pixels). The remaining gradient is related to the fact that the source image is lower than 50% on the right hand side.
- The histogram shows a peak with very few different gray values.

Loading a shading image out of the camera

GPDATA_BUFFER is used to load a shading image out of the camera. Because the size of a shading image is larger than GPDATA_BUFFER, input must be handled in several steps:

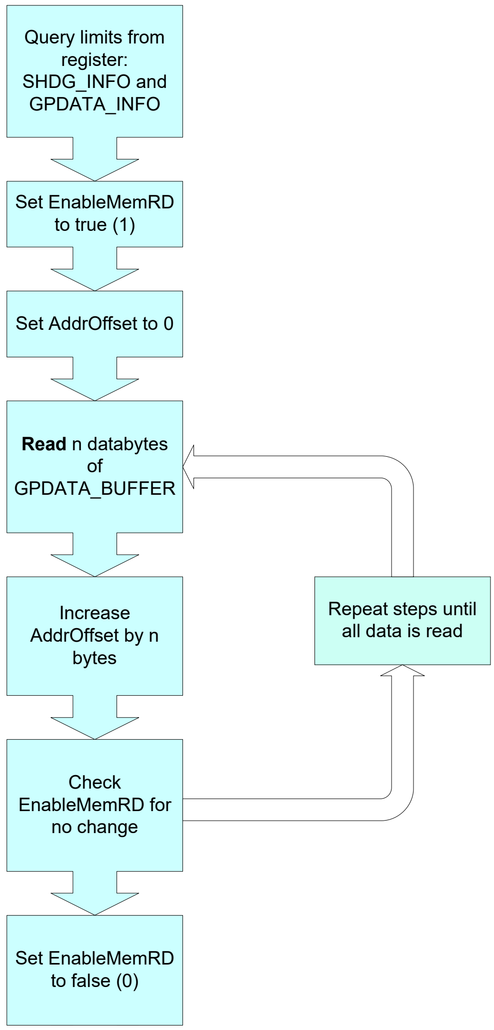


Figure 47: Uploading shading image to host

Note

Configuration

- To configure this feature in an advanced register, see Table 164: Advanced register: Shading on page 302.
- For information on GPDATA_BUFFER, see GPDATA_BUFFER on page 335.

Loading a shading image into the camera

GPDATA_BUFFER is used to load a shading image into the camera. Because the size of a shading image is larger than GPDATA_BUFFER, input must be handled in several steps (see also Reading or writing shading image from/into the camera on page 303).

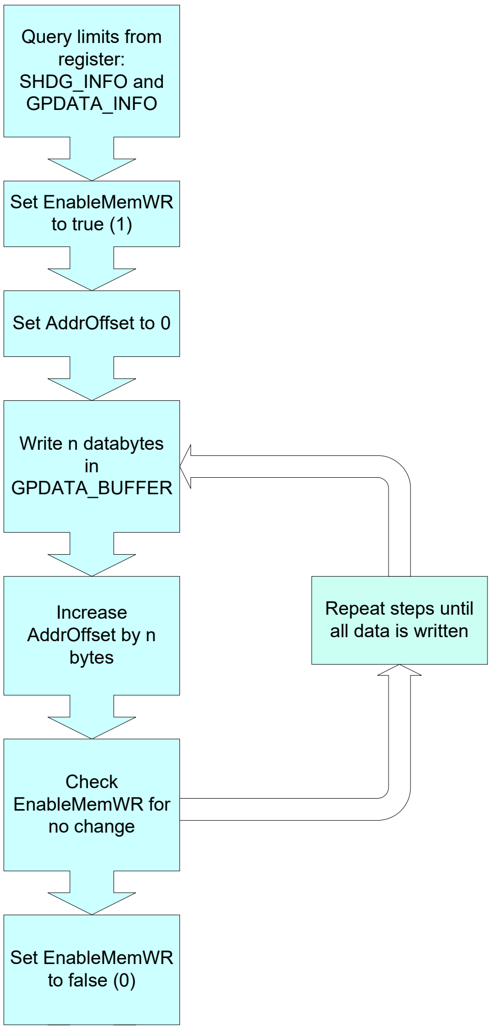


Figure 48: Loading the shading reference image

Note

Configuration

- To configure this feature in an advanced register, see Table 164: Advanced register: Shading on page 302.
- For information on GPDATA_BUFFER, see GPDATA_BUFFER on page 335.

Look-up table (LUT) and gamma function

The Pike camera provides sixteen (0-15) user-defined look-up tables (LUT). The use of one LUT allows any function (in the form Output = F(Input)) to be stored in the camera's RAM and to be applied on the individual pixels of an image at run-time.

The address lines of the RAM are connected to the incoming digital data, these in turn point to the values of functions which are calculated offline, e.g. with a spreadsheet program.

This function needs to be loaded into the camera's RAM before use.

One example of using an LUT is the gamma LUT:

There are two gamma LUTs (gamma=0.7 and gamma=0.45)

Output = $(\text{Input})^{0.7}$ and Output = $(\text{Input})^{0.45}$

These two gamma LUTs are used with all Pike models.

Gamma is known as compensation for the nonlinear brightness response of many displays e.g. CRT monitors. The look-up table converts the incoming **14 bit** from the digitizer to outgoing up to **14-bit**.

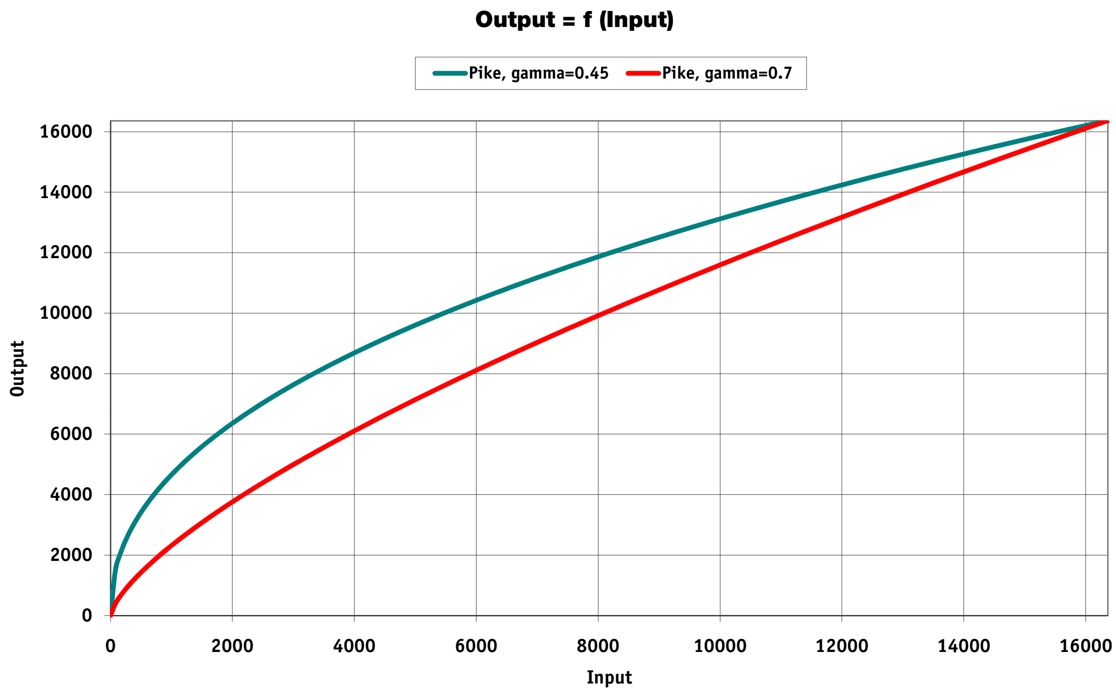


Figure 49: LUTs with gamma=0.45, gamma=0.7

Note

- The input value is the **14-bit** value from the digitizer.
- The two gamma LUTs use LUT 14 and 15.
- Gamma 1 (gamma=0.7) switches on LUT 14, gamma 2 (gamma=0.45) switches on LUT 15. After overriding LUT 14 and 15 with a user defined content, gamma functionality is no longer available until the next full initialization of the camera.
- LUT content is volatile if you do not use the user profiles to save the LUT.

Loading an LUT into the camera

Loading the LUT is carried out through the data exchange buffer called GPDATA_BUFFER. As this buffer can hold a maximum of 2 KB, and a complete LUT at **16384 × 14-bit** is **28 KB**, programming can not take place in a one block write step because the size of an LUT is larger than GPDATA_BUFFER. Therefore input must be handled in several steps. The flow diagram below shows the sequence required to load data into the camera.

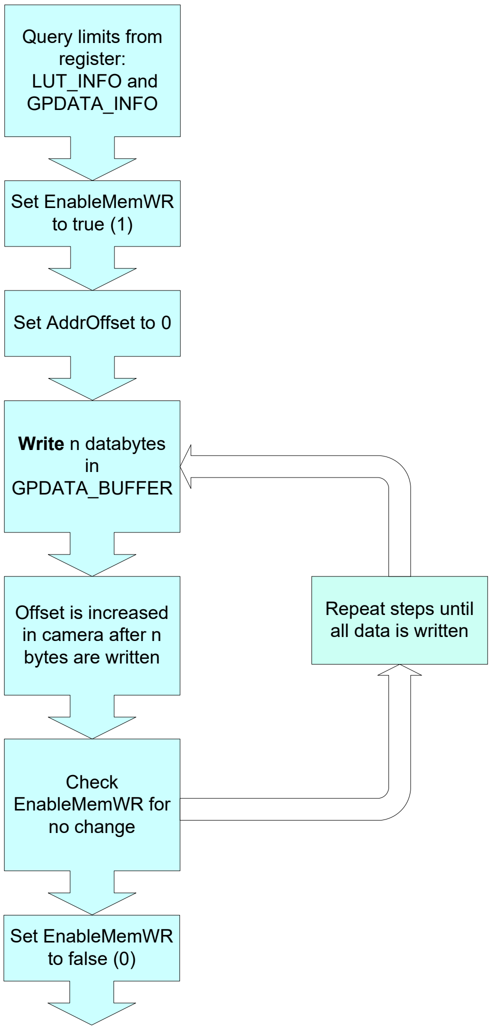


Figure 50: Loading an LUT

Note

Configuration

- To configure this feature in an advanced register, see Table 163: Advanced register: LUT on page 300.
- For information on GPDATA_BUFFER, see GPDATA_BUFFER on page 335.

Defect pixel correction (Pike F-1100, F-1600 only)

ON Semiconductor sensors for Pike F-1100, F-1600 are delivered with standard class 2 sensors, which allow certain types of defect pixels according to the following ON Semiconductor definitions.

Defect pixel definitions for Pike F-1100

The following defect pixel definitions are according data sheet for ON Semiconductor KAI-11002.

Description	Definition	Class X Monochrome with microlens only	Class 0 Monochrome with microlens only	Class 1	Class 2 Color only	Class 2 Monochrome only
Major dark field defect pixel	Defect ≥ 239 mV	100	100	100	200	200
Major bright field defect pixel	Defect ≥ 15%					
Minor dark field defect pixel	Defect ≥ 123 mV	1000	1000	1000	2000	2000
Cluster defect	A group of 2 to N contiguous major defect pixels, but no more than W adjacent defects horizontally.	0	1 N=10 W=3	20 N=10 W=3	20 N=10 W=3	20 N=12 W=5
Column defect	A group of more than 10 contiguous major defect pixels along a single column.	0	0	0	10	2

Table 50: Defect pixel definitions: Pike F-1100 (ON Semiconductor KAI-11002 sensors)

Defect pixel definitions for Pike F-1600

The following defect pixel definitions are according data sheet for ON Semiconductor KAI-16000.

Description	Definition	Class 1	Class 2 Monochrome only	Class 2 Color only
Major dark field defect pixel	Defect ≥ 245 mV	150	300	300
Major bright field defect pixel	Defect ≥ 15%			
Minor dark field defect pixel	Defect ≥ 126 mV	1500	3000	3000
Cluster defect	A group of 2 to N contiguous major defect pixels, but no more than W adjacent defects horizontally.	30 N=20 W=4	30 N=20 W=4	30 N=20 W=4
Column defect	A group of more than 10 contiguous major defect pixels along a single column.	0	4	15

Table 51: Defect pixel definitions: Pike F-1600 (ON Semiconductor KAI-16000 sensors)

Allied Vision factory default settings

For each ON Semiconductor 11 Megapixel and 16 Megapixel sensor, ON Semiconductor provides a defect pixel map according to their specifications, see Defect pixel definitions for Pike F-1100 on page 132 and Defect pixel definitions for Pike F-1600 on page 133.

The customer can see these defect pixel values via SmartView. It's recommended to make a backup of the factory default defect pixel map by saving this file via Smart view **before** adding some changes to the list, see Defect pixel editor in SmartView on page 134.

Allied Vision defect pixel map

Allied Vision has defined its own defect pixel list format. This results in the following advantages:

Advantages of the Allied Vision-own defect pixel map:

- You can specify partial columns instead of whole columns.
- You can use coordinates from final camera image: same as used e.g. in SmartView.
- You can use a CSV file format. Therefore also common spread-sheet applications like Microsoft Excel can be used as external editors.

This is an example file of the Allied Vision-own defect pixel map format: Values are separated by semicolon:

```
X; Y; Height
3440;39;132
```

```
890;2157;1
891;2157;1
1724;752;1
1725;752;1
1726;753;1
1724;753;1
75;2165;1
137;2486;1
2120;1384;1
14;38;1
```

X and Y coordinates show single defect pixel, if Height = 1.

X and Y coordinates show a column defect, if Height ≥ 1.

Number of lines starting at position (this is only true in Format_7 Mode_0 and with full AOI):

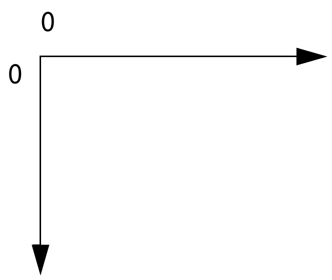


Figure 51: Coordinate system

Defect pixel editor in SmartView

With SmartView 1.13 or greater you can edit the defect pixels directly in the camera (**Adv 4** tab).

Info

We strongly recommend to make a backup of the factory default settings. Therefore save the defect pixel map (stored in the camera) into a csv file, before making any changes.

If you delete one or several pixels (or if you make any manipulations of the defect pixel list), you will loose the original defect pixel list.

Starting the camera or SmartView **does not** initiate the download of the defect pixel list.

To download the defect pixel data from the camera into SmartView defect pixel editor: open the defect pixel editor dialog (Adv4 tab, see screenshot below).

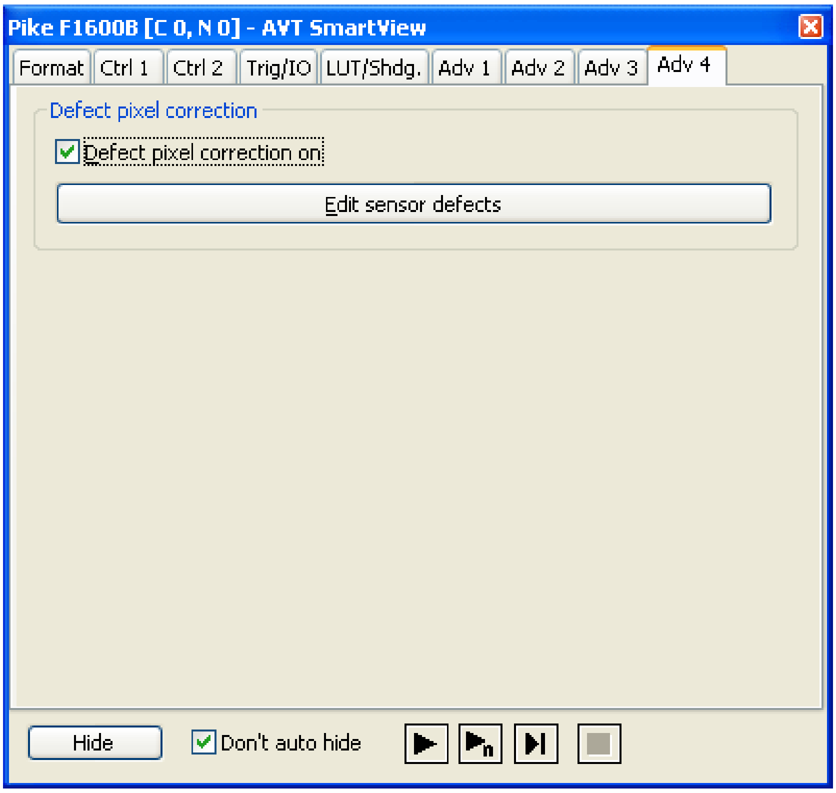


Figure 52: SmartView: Adv 4 tab: Defect pixel correction

Features:

- Upload from SmartView to the camera.
- Download from the camera to SmartView.
- Activate/Deactivate defect pixel correction (factory default setting: activated on startup of SmartView)
- Save/load of Allied Vision-own defect pixel map for external use
- Displaying current defect pixels of the camera
- Add/remove defect pixels

With an upload to and download from the camera you can manipulate the defect data stored in the camera. Additionally you can activate and deactivate defect pixel correction entirely.

Section	Check box / button/ combo box/ list / slider	Description
Defect pixel correction	☑Defect pixel correction on	Activate check box for applying defect pixel correction. **Note:** This check box is not activated on SmartView startup in general. Activation of DPC is factory default for the camera. Setting of the check box is only dependent on current setting in the camera, but not on startup of SmartView.
	Edit sensor defects	Loads current defect pixel data into the camera and opens the Defect pixel editor in SmartView.

Table 52: SmartView Edit settings: Adv 4 tab (Defect pixel correction)

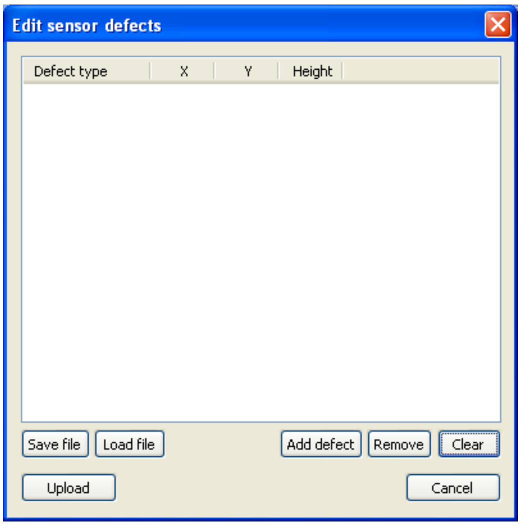
Editor	Check box / buttons	Description
Edit defect pixels		
	Save file	Saves defect pixel data in a CSV file (Allied Vision -own defect pixel file).
	Load file	An **Open** dialog opens. Choose the following file type: • Allied Vision defect files (*.csv) [defect values are loaded into the **Edit sensor defects** dialog]
	Add defect	Here you can add more defect pixels manually. For a single defect pixel enter X and Y value. For a column enter X value only (whole column defect) or X and Y value and height (partial column defect).
	Remove	Mark one or more defect pixels and click **Remove** to delete defect pixels.
	Clear	Deletes all defect pixels from the editor.
	Upload	Changed defect pixel data are loaded into the camera. If you clicked **Clear**, the defect pixel map in the camera is deleted. We strongly recommend to save the defect pixel map (stored in the camera) into a csv file, before uploading data.
	Cancel	Cancels all actions done in the editor.

Table 53: SmartView Edit settings: Adv 4 tab (Defect pixel correction editor)

Defect Pixel editor: more details

Some reasons why you should use the editor:

- Depending on the environment conditions where the camera is used, it may happen that more defect pixels will occur. This depends on the operation time of the camera/sensor. In that case you are able to add new identified defect pixels to the list.
- The ON Semiconductor defect pixel file, used as the factory setting, lists the whole column as a defect column, although there may be only 10 or more defect pixels in this column. In this case you can define the real defect pixels.

To edit defect pixels in **Edit sensor defects** dialog manually:

1. Double-click defect pixel value or click **Add defect**.

   Add defect dialog opens.

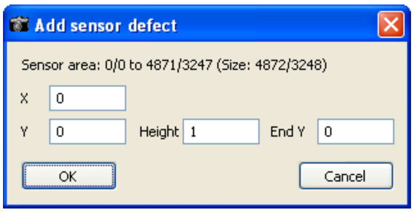


Figure 53: **Add defect** *dialog*

2. For a single defect pixel: Enter **X** and **Y** coordinates.
   For adjacent defect pixels in a column: Enter **X** and **Y** for starting point and **End Y** for the last of the adjacent defect pixels in this column. The height will be calculated automatically.

The defect pixels are stored non-volatile in the camera, when you click **Upload** in the **Edit sensor defects** dialog.

Where is the defect pixel correction done?

Defect pixel correction is done in the FPGA.

Note

Configuration

- To configure this feature in an advanced register, see Defect pixel correction on page 329.

Binning (monochrome models only)

2 ×, 4 ×, 8 × binning

Definition

Binning is the process of combining neighboring pixels while being read out from the CCD chip.

Note

- Only monochrome Pike cameras have this feature.
- Binning does not change offset, brightness or blacklevel.

Binning is used primarily for 3 reasons:

- A reduction in the number of pixels; thus, the amount of data while retaining the original image area angle
- An increase in the frame rate (vertical binning only)
- A brighter image, resulting in an improvement in the signal-to-noise ratio of the image (depending on the acquisition conditions)

Signal-to-noise ratio (SNR) and **signal-to-noise separation** specify the quality of a signal with regard to its reproduction of intensities. The value signifies how high the ratio of noise is in regard to the maximum achievable signal intensity.

The higher this value, the better the signal quality. The unit of measurement used is generally known as the decibel (dB), a logarithmic power level. 6 dB is the signal level at approximately a factor of 2.

However, the advantages of increasing signal quality are accompanied by a reduction in resolution.

Format_7 only

Binning is possible only in video Format_7. The type of binning used depends on the video mode.

Note

Changing binning modes involves the generation of new shading reference images due to a change in the image size.

Types

In general, we distinguish between the following types of binning (H=horizontal, V=vertical):

- 2 × H-binning
- 2 × V-binning
- 4 × H-binning
- 4 × V-binning
- 8 × H-binning
- 8 × V-binning

and the full binning modes:

- 2 × full binning (a combination of 2 × H-binning and 2 × V-binning)

- 4 × full binning (a combination of 4 × H-binning and 4 × V-binning)
- 8 × full binning (a combination of 8 × H-binning and 8 × V-binning)

Vertical binning

Vertical binning increases the light sensitivity of the camera by a factor of two (4 or 8) by adding together the values of two (4 or 8) adjoining vertical pixels output as a single pixel. This is done directly in the horizontal shift register of the sensor.

Format_7 Mode_2 By default and without further remapping use **Format_7 Mode_2** for 2 × vertical binning.

This reduces vertical resolution, depending on the model.

Figure 54: 2 × vertical binning and 4 × vertical binning

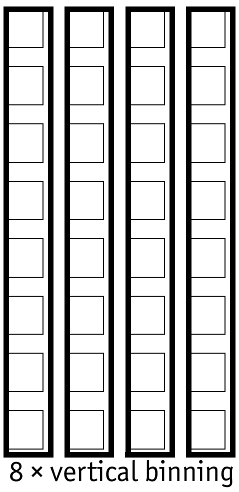


Figure 55: 8 × vertical binning

Note

Vertical resolution is reduced, but **signal-to noise ratio** (SNR) is increased by about 3, 6 or 9 dB (2 ×, 4 × or 8 × binning).

Note

If **vertical binning** is activated the image may appear to be over-exposed and may require correction.

Note

The image appears **vertically** compressed in this mode and no longer exhibits a true aspect ratio.

Horizontal binning

In horizontal binning adjacent horizontal pixels in a line are combined digitally in the FPGA of the camera without accumulating the black level:

2 × horizontal binning: 2 pixel signals from 2 horizontal neighboring pixels are combined.

4 × horizontal binning: 4 pixel signals from 4 horizontal neighboring pixels are combined.

8 × horizontal binning: 8 pixel signals from 8 horizontal neighboring pixels are combined.

Light sensitivity

This means that in horizontal binning the **light sensitivity** of the camera is also increased by a factor of two (**6 dB**), 4 (**12 dB**) or 8 (**18 dB**). Signal-to-noise separation improves by approx. 3, 6 or 9 dB.

Horizontal resolution

Horizontal resolution is lowered, depending on the model.

Format_7 Mode_1

By default and without further remapping use **Format_7 Mode_1** for 2 × horizontal binning.

Figure 56: 2 × horizontal binning and 4 × horizontal binning

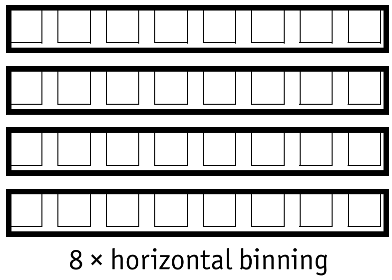


Figure 57: 8 × horizontal binning

Note

The image appears **horizontally** compressed in this mode and does no longer show true aspect ratio.

If **horizontal binning** is activated the image may appear to be over-exposed and must eventually be corrected.

2 × full binning, 4 × full binning, 8 × full binning

If horizontal and vertical binning are combined, every 4 (16 or 64) pixels are consolidated into a single pixel. At first two (4 or 8) vertical pixels are put together and then combined horizontally.

This increases light sensitivity by a total of a factor of 4 (16 or 64) and at the same time signal-to-noise separation is improved by about 6 (12 or 18) dB. Resolution is reduced, depending on the model.

By default and without further remapping use **Format_7 Mode_3** for 2 × full binning.

Figure 58: 2 × and 4 × full binning

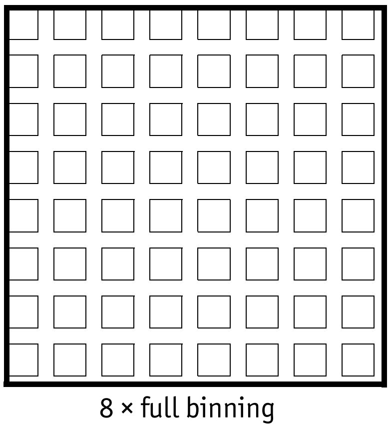


Figure 59: 8 × full binning

Sub-sampling (monochrome and color models)

What is sub-sampling?

Definition Sub-sampling is the process of skipping neighboring pixels (with the same color) while being read out from the CCD chip.

Which models have sub-sampling?

All Pike models, both color and monochrome, have this feature.

Description of sub-sampling

Sub-sampling is used primarily for the following reason:

- A reduction in the number of pixels and thus the amount of data while retaining the original image area angle and image brightness

Similar to binning mode the cameras support horizontal, vertical and h+v sub-sampling mode.

Format_7 Mode_4 By default and without further remapping use **Format_7 Mode_4** for

- monochrome models: 2 out of 4 horizontal sub-sampling
- color models: 2 out of 4 horizontal sub-sampling

The different sub-sampling patterns are shown below.

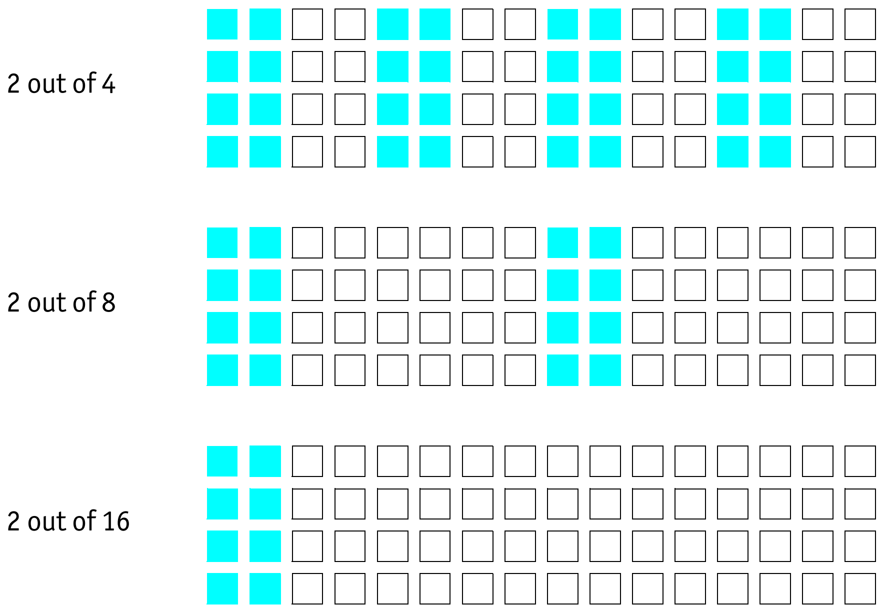


Figure 60: Horizontal sub-sampling (monochrome)

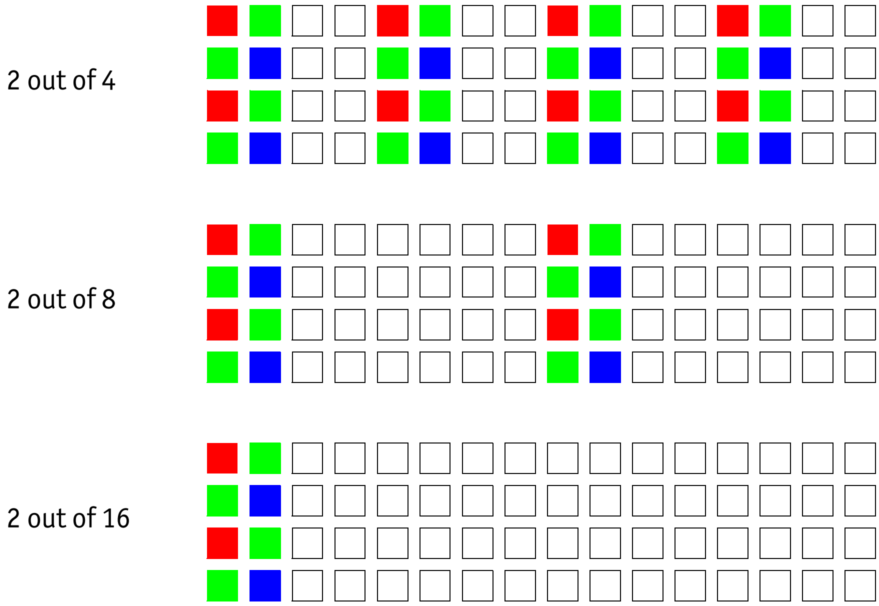


Figure 61: Horizontal sub-sampling (color)

Note

The image appears **horizontally compressed** in this mode and no longer exhibits a true aspect ratio.

Format_7 Mode_5

By default and without further remapping use **Format_7 Mode_5** for

- **monochrome** models: 2 out of 4 vertical sub-sampling
- **color** models: 2 out of 4 vertical sub-sampling

The different sub-sampling patterns are shown below.

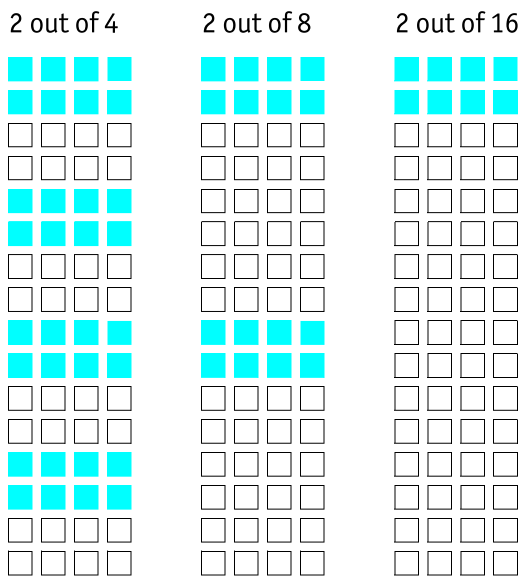


Figure 62: Vertical sub-sampling (monochrome)

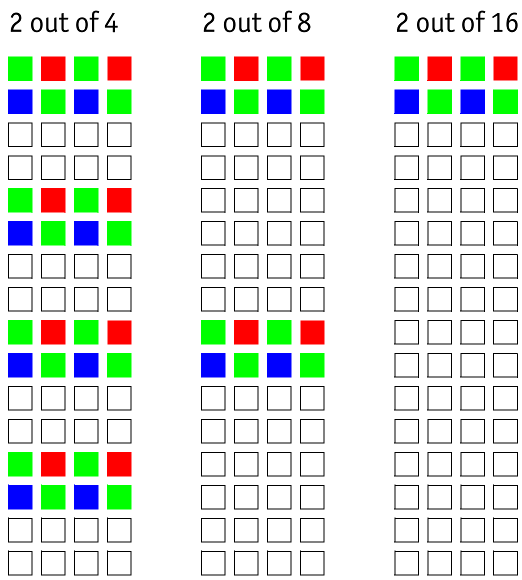


Figure 63: Vertical sub-sampling (color)

Note

The image appears vertically compressed in this mode and no longer exhibits a true aspect ratio.

Format_7 Mode_6

By default and without further remapping use **Format_7 Mode_6** for 2 out of 4 H+V sub-sampling

The different sub-sampling patterns are shown below.

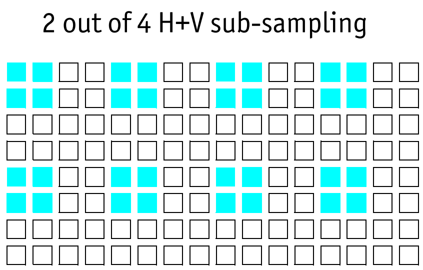


Figure 64: 2 out of 4 H+V sub-sampling (monochrome)

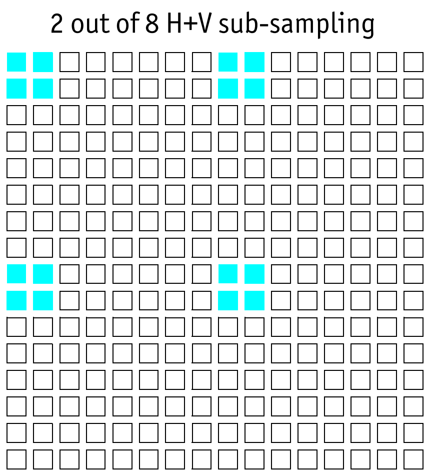


Figure 65: 2 out of 8 H+V sub-sampling (monochrome)

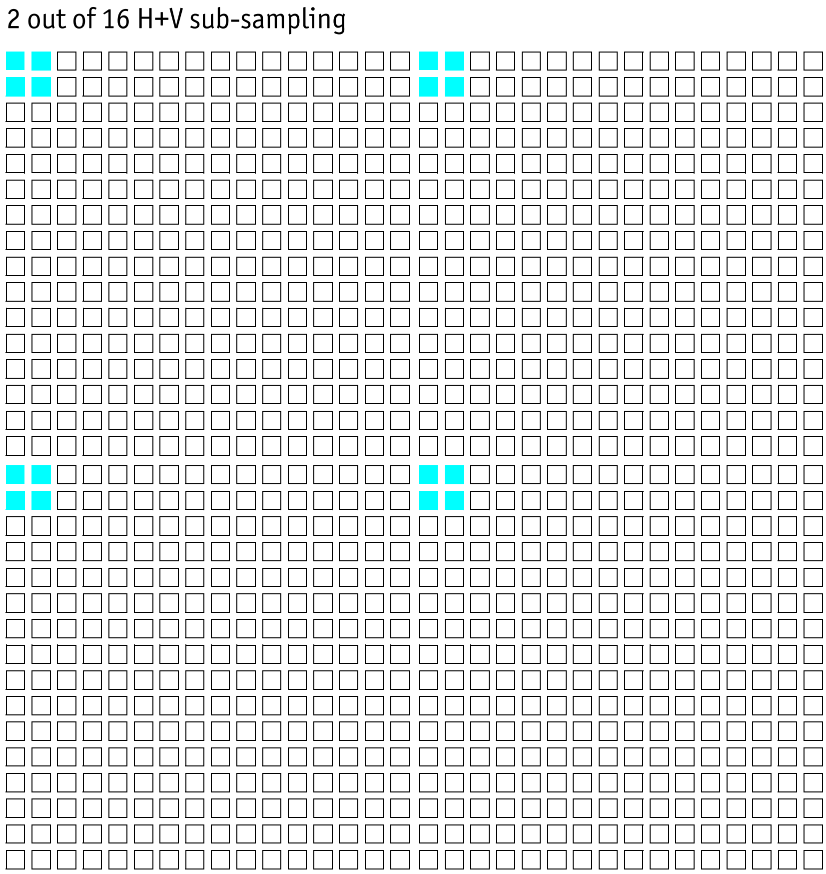


Figure 66: 2 out of 16 H+V sub-sampling (monochrome)

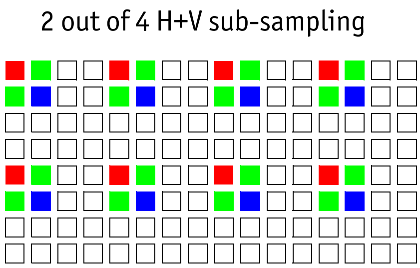


Figure 67: 2 out of 4 H+V sub-sampling (color)

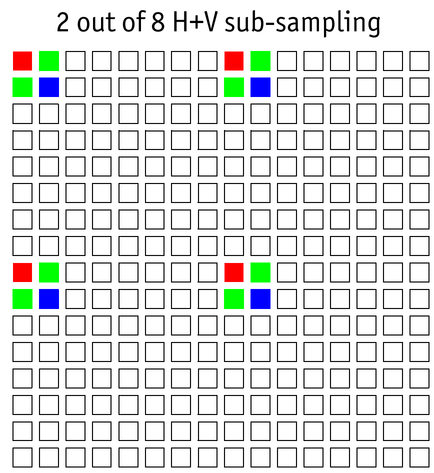


Figure 68: 2 out of 8 H+V sub-sampling (color)

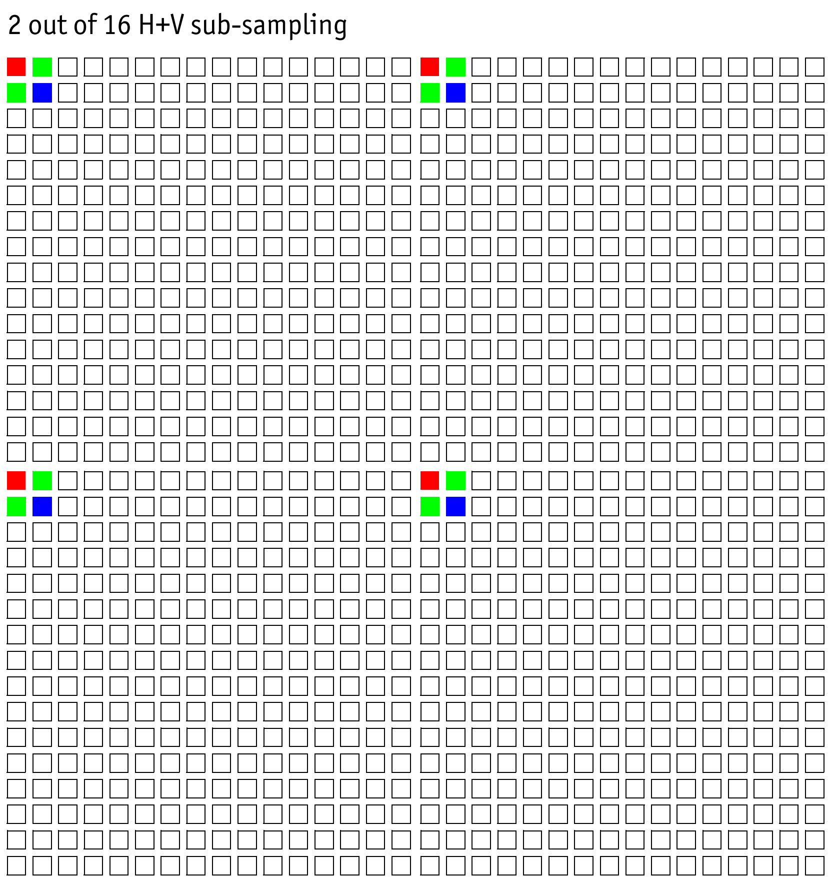


Figure 69: 2 out of 16 H+V sub-sampling (color)

Note

Changing sub-sampling modes involves the generation of new shading reference images due to a change in the image size.

Binning and sub-sampling access

The binning and sub-sampling modes described in the last two chapters are only available as pure binning or pure sub-sampling modes. A combination of both is not possible.

As you can see there is a vast amount of possible combinations. But the number of available Format_7 modes is limited and lower than the possible combinations.

Thus access to the binning and sub-sampling modes is implemented in the following way:

- Format_7 Mode_0 is fixed and can not be changed
- A maximum of 7 individual Allied Vision modes can be mapped to Format_7 Mode_1 to Mode_7 (see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152)
- Mappings can be stored via register (see Format_7 mode mapping on page 322) and are uploaded automatically into the camera on camera reset.
- The **default settings** (per factory) in the Format_7 modes are listed in the following table

Format_7	Pike monochrome models: Format_7	Pike color models: Format_7
Mode_0	full resolution, no binning, no sub-sampling	full resolution, no sub-sampling
Mode_1	2 × **horizontal** binning	---
Mode_2	2 × **vertical** binning	---
Mode_3	2 × **full** binning	---
Mode_4	2 out of 4 **horizontal** sub-sampling	2 out of 4 **horizontal** sub-sampling
Mode_5	2 out of 4 **vertical** sub-sampling	2 out of 4 **vertical** sub-sampling
Mode_6	2 out of 4 **full** sub-sampling	2 out of 4 **full** sub-sampling

Table 54: Default Format_7 binning and sub-sampling modes (per factory settings)

Note

- A **combination** of binning and sub-sampling modes is **not possible**.
  Use either pure binning or pure sub-sampling modes.
- The Format_ID numbers 0 to 31 in the binning / sub-sampling list do **not** correspond to any of the Format_7 modes.

F7 modes according to IIDC 1394

F7M0 (no change)
F7M1
F7M2
F7M3
F7M4
F7M5
F7M6
F7M7

mapping of each of 32 modes to F7M1..F7M7 possible

Format_ID (see p322)Allied Vision modes

0	0 × horizontal	0 × vertical	binning (only monochrome cameras)
1	2 × horizontal		
2	4 × horizontal		
3	8 × horizontal		
4	0 × horizontal	2 × vertical	
5	2 × horizontal		
6	4 × horizontal		
7	8 × horizontal		
8	0 × horizontal	4 × vertical	
9	2 × horizontal		
10	4 × horizontal		
11	8 × horizontal		
12	0 × horizontal	8 × vertical	
13	2 × horizontal		
14	4 × horizontal		
15	8 × horizontal		
16	---	2 out of 2 vertical	sub-sampling (color and monochrome)
17	2 out of4horizontal		
18	2 out of8horizontal		
19	2 out of16horizontal		
20	2 out of2horizontal	2 out of 4 vertical	
21	2 out of4horizontal		
22	2 out of8horizontal		
23	2 out of16horizontal		
24	2 out of2horizontal	2 out of 8 vertical	
25	2 out of4horizontal		
26	2 out of8horizontal		
27	2 out of16horizontal		
28	2 out of2horizontal	2 out of 16 vertical	
29	2 out of4horizontal		
30	2 out of8horizontal		
31	2 out of16horizontal		

Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7

Note

Configuration

To configure this feature in an advanced register, see Table 186: Advanced register: Format_7 mode mapping on page 322.

Quick parameter change timing modes

Why new timing modes?

Former timing of the Pike cameras showed the same behavior as Marlin cameras:

- Frame rate or transfer rate is always constant (precondition: shutter < transfer time)
- The delay from shutter update until the change takes place: up to 3 frames. Figure 71: Former standard timing on page 153 demonstrates this behavior. It shows that the camera receives a shutter update command while the sensor is currently integrating (Sync is low) with shutter setting 400. The camera continues to integrate and this image is output with the next FVal. The shutter change command becomes effective with the next falling edge of sync and finally the image taken with shutter 200 is output with a considerable delay.
- Parameters that are sent to the camera faster than the maximum frame rate per second are stored in a FIFO and are activated in consecutive images.

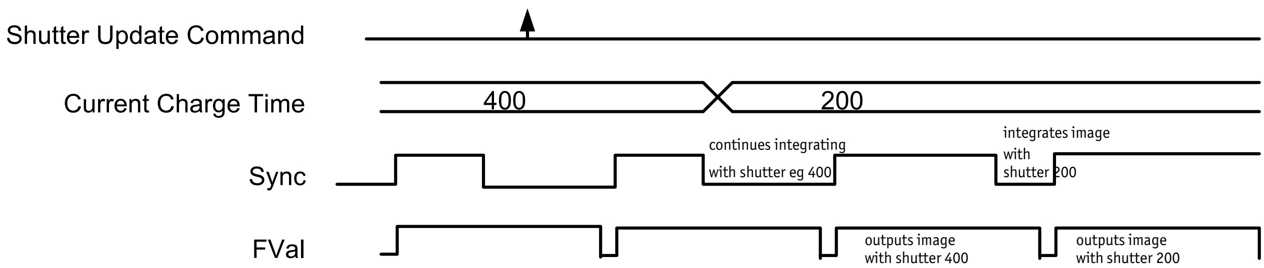


Figure 71: Former standard timing

Principally a Pike camera is not able to recognize how many parameter the user will change. Due to the fact that communication between host and camera is asynchronous, it may happen that one part of parameter changes is done in image n+1 and the other part is done in image n+2.

To optimize the transfer of parameter changes there is a new timing mode called Quick Format Change Mode, which effectively resets the current shutter.

Therefore you can choose between the following update timing modes:

- Standard Parameter Update Timing (slightly modified from previous Pike cameras)
- New: Quick Format Change Mode

In the following you find a short description of both timing modes:

Standard Parameter Update Timing

The Standard Parameter Update Timing keeps the frame rate constant and does not create any gaps between two image transfers via bus (precondition: exposure (shutter) time must be smaller than transfer time).

- Frame rate / transfer rate is always constant
  (if shutter time < transfer time)
- Delay from shutter update until change takes place is always 2 frames (delay from update command reception by FPGA and not by microcontroller)
- Parameters sent to the camera faster than maximum frame rate are no longer stored in a FIFO. The last sent parameter will be activated for the next image. All others will be dropped. This ensures that the last image is shot with the last shutter setting.

New: Quick Format Change Mode (QFCM)

The Quick Format Change Mode creates gaps between two images. Current exposure is interrupted and the new exposure is started immediately with new parameters if during exposure (integration/shutter) an new shutter command is received.

- Frame rate / transfer rate can be *interrupted.* This is shown in the diagram below whenever FVal goes low after a reception of a new shutter command while Sync was low.
- Shutter will be interrupted, if the update command is received while camera integrates
- Delay from shutter update until change takes place is always 1 frame (the delay is calculated from update command reception by FPGA and not by microcontroller)

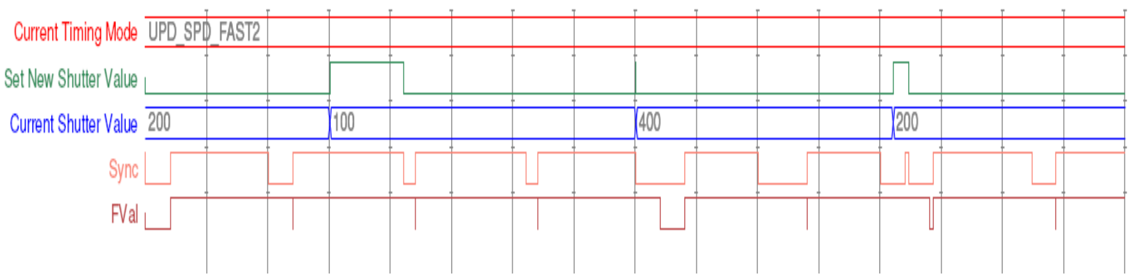


Figure 72: Quick Format Change Mode

How to transfer parameters to the camera

The following 3 variants of transferring the parameters are available with the firmware 3.x:

Transfer mode	Advantage	Disadvantage
Encapsulated Update (begin/end)	• easy to use (standard quad writes in camera register is possible)	• one write access per register access
Parameter-List Update	• only one write access for all parameters • fastest host→camera transfer (from 5 parameters on faster than encapsulated mode) • handling of parameter list is easy	• not so easy to use (block writes) • maximum 64 entries for parameter list
Standard Update (IIDC)	• compliant with IIDC V1.31	• non deterministic change of parameters

Table 55: Comparison of three transfer modes

In the following you find a short description of each variant:

Encapsulated Update (begin/end)

The Encapsulated Update (begin/end) has the following characteristics:

- Host will set a parameter update begin flag in the camera (UpdActive Field in Register 0xF1000570, see Table 181: Advanced register: Update timing modes on page 318)
- Host will send several parameters to the camera and then signalize end by resetting the flag
- All parameters will become active for the same next image
- Dependent on timing mode, the camera
  - (standard Update): uses the previous parameters until the update flag (UpdActive Field in Register 0xF1000570) is reset
  - (Quick Format Change Mode): Camera stops and waits until the update flag (UpdActive Field in Register 0xF1000570) is reset.

In the Encapsulated Update (begin/end) the exact sequence is:

1. Parameter update begin (advanced feature register)
2. Standard IIDC register update (1..N register) (standard feature register)
3. Parameter update end (advanced feature register)

Camera timing behavior is described in the following table.

After the parameter update stop command all changed parameters are valid for the available next image. Frame rate is constant.	After the parameter update start command a current transfer is interrupted. A started exposure will be interrupted until the next parameter update stop command. Exposure of the next image with new parameters is started. There may be a gap between two succeeding images but images are always transmitted completely.

Table 56: Encapsulated Update (begin/end)*: comparison of standard timing and fast timing 2*

If after end of time-out (10 seconds after Quick Format Change Mode) no **parameter update end** is sent, all changes will become valid.

A new write event of **parameter update begin** starts time-out again.

Parameter-List Update

In the Parameter-List Update mode a complete list with IIDC addresses and values of up to 64 parameters is sent to the camera.

- Host sends a list with parameters to the camera (advanced feature space)
- Microcontroller processes that list
- All parameters will become active for the same image
- Dependent on timing mode, the camera will:
  - Standard Format Change Mode: use the previous parameters until the new parameter set is copied to the FPGA
  - Quick Format Change Mode (QFCM): waits until all parameters have been copied to the FPGA and may interrupt an already started integration for a new integration with the new settings

Example of parameter list is described in the following table.

Address	Value
0xF0F0081C	0x80000100
0xF0F00820	0x800000ac
0xF0F00818	0x82000001
...	...

Table 57: Example of parameter list

The exact sequence is:

Block-write (this needs to be a functionality of the underlying software stack (e.g. FirePackage). It may not be available for third party IIDC software stacks.) of list to advanced feature address

Camera timing is described in the following table.

After block write command is processed in the camera all changed parameters are valid for the available next image. Frame rate is constant.	After transfer of the parameter list via block write a current transfer will be finished. A started exposure will be interrupted until the microcontroller has processed the list and copied it into the FPGA. Exposure of the next image with new parameters is started. There may be a gap between two images.

Table 58: Parameter-List Update*: comparison of standard timing and* QFCM

Standard Update (IIDC)

In the Standard Update (IIDC) mode single parameter are sent to the camera.

- Standard Update (IIDC)shows same behavior as Marlin
- Parameter will be sent from host to camera and will be activated as soon as possible without interruption of the transfer
- If the host updates more than one parameter (without block write) the parameters may become active in different images
- Standard Update (IIDC) can be combined with the new parameter update timing modes

Camera timing behavior is described in the following table.

After sending a new parameter value, the changed parameter value is valid for the available next image. Frame rate is constant.	After sending a new parameter value, the changed parameter value is valid for the available next image. A running exposure will be interrupted and the image is dropped. There may be a gap between two consecutive image transfers.

Table 59: Standard Update (IIDC)*: comparison of* Standard Format Change Mode *and* QFCM

Packed 12-Bit Mode

All Pike cameras have the so-called Packed 12-Bit Mode. This means: two 12-bit pixel values are packed into 3 bytes instead of 4 bytes.

B/w cameras	Color cameras
Packed 12-Bit MONO camera mode SmartView: MONO12	Packed 12-Bit RAW camera mode SmartView: RAW12
Mono and raw mode have the same implementation.	

Table 60: Packed 12-Bit Mode

Note

For data block packet format see Table 40: Packed 12-Bit Mode (mono and raw) Y12 format (Allied Vision) on page 99.

For data structure see Table 41: Data structure of Packed 12-Bit Mode (mono and raw) (Allied Vision) on page 101.

The color codings are implemented via Vendor Unique Color_Coding according to IIDC V1.31: COLOR_CODING_INQ @ 024h to 033h, IDs=128-255)

See Table 152: Format_7 control and status register on page 285.

Mode	Color_Coding	ID
Packed 12-Bit MONO	ECCID_MONO12	ID=132
Packed 12-Bit RAW	ECCID_RAW12	ID=136

Table 61: Packed 12-Bit Mode*: color coding*

High SNR mode (High Signal Noise Ratio)

Note

Configuration

To configure this feature in an advanced register, see Table 178: Advanced register: High Signal Noise Ratio (HSNR) on page 315.

In this mode the camera grabs and averages a set number of images and outputs one image with the same bit depth and the same brightness. This means that the camera will output an 8-bit averaged image when an 8-bit image format is selected (although the internal calculations are done with 14-bit).

Because of the fact that normally uncorrelated (photon-, amplifier-) noise dominates over correlated noise (fixed pattern noise), adding two images will double (6 dB) the gray levels but only increase the noise levels by $\sqrt{2}$ (3 dB).

This enhances both the dynamic range as well as the signal-to-noise ratio.

Consequently adding 256 8-bit images will lead to a potential signal-to-noise enhancement of 24 dB or a resulting bit depth of 16 bit.

Note

- The camera must be idle to toggle this feature on/off. Idle means: no image acquisition, no trigger.
- Set grab count and activation of HighSNR in **one single write access**.

Note

- The averaged image is output at a lower frame rate roughly equivalent to fps_old/N, where N is the number of images averaged. In fact, due to camera internal conditions, and according to which format and mode settings are in use, it can vary slightly to be closer sometimes to 1/ ((N/fps_old) + T_shutter). It's impractical to express in a formula or tables, across all camera models and modes. But these notes should be sufficient to help each user determine that the camera behaves as described.
- The potential SNR enhancement may be lower when using more than 8-bit original bit depth.
- Select 16-bit image format in order to take advantage of the full potential SNR and DNR (**D**y**N**amic **R**ange) enhancements.
- For 8-bit video modes, the internal HSNR calculations are done with 14-bit.

Frame memory and deferred image transport

An image is normally captured and transported in consecutive steps. The image is taken, read out from the sensor, digitized and sent over the IEEE1394 bus.

Deferred image transport

As all Pike cameras are equipped with built-in image memory, this order of events can be paused or delayed by using the **deferred image transport** feature.

Pike cameras are equipped with 64 MB of RAM (Pike F-1100, F-1600: 256 MB). The table below shows how many frames can be stored by each model. The memory operates according to the FIFO (first in, first out) principle. This makes addressing for individual images unnecessary.

Model	Memory size
Pike F-032B, F-032C Pike F-032B, F-032C fiber	105 frames
Pike F-100B, F-100C Pike F-100B, F-100C fiber	32 frames
Pike F-145B, F-145C Pike F-145B, F-145C fiber	22 frames
Pike F-145B, F-145C-15fps Pike F-145B, F-145C fiber-15fps	22 frames
Pike F-210B Pike F-210B fiber	15 frames
Pike F-421B, F-421C Pike F-421B, F-421C fiber	6 frames
Pike F-505B, F-505C Pike F-505B, F-505C fiber	5 frames
Pike F-1100B, F-1100C Pike F-1100B, F-1100C fiber	11 frames
Pike F-1600B, F-1600C Pike F-1600B, F-1600C fiber	7 frames

Table 62: Image buffer memory size

Deferred image transport is especially useful for multi-camera applications:

Assuming several cameras acquire images concurrently. These are stored in the built-in image memory of every camera. Until this memory is full, the limiting factor of available bus bandwidth, DMA- or ISO-channel is overcome.

Image transfer is controlled from the host computer by addressing individual cameras one after the other and reading out the desired number of images.

Note

Configuration

To configure this feature in an advanced register, see Table 166: Advanced register: Deferred image transport on page 305.

HoldImg mode

By setting the **HoldImg** flag, transport of the image over the IEEE1394 bus is stopped completely. All captured images are stored in the internal **ImageFiFo**. The camera reports the maximum possible number of images in the **FiFoSize** variable.

Note

- Pay attention to the maximum number of images that can be stored in the **image buffer**. If you capture more images than the number in **FiFoSize**, the oldest images are overwritten.
- The extra **SendImage** flag is set to **true** to import the images from the camera. The camera sends the number of images set in the **NumOfImages** parameter.
- If **NumOfImages** is **0,** all images stored in the image buffer will be sent.
- If **NumOfImages** is not **0**, the corresponding number of images will be sent.
- If the **HoldImg** field is set to **false**, all images in **ImageFIFO** will be deleted. No images will be sent.
- The last image in the image buffer will be corrupted, when simultaneously used as input buffer while being read out. In this case read out one image less than maximum buffer size.
- **NumOfImages** is incremented after an image was read out of the sensor and therefore stored into the onboard image buffer.
- **NumOfImages** is decremented after the last isochronous packet of an image was handed over to the IEEE1394 chipset of the camera.

The following screenshot shows the sequence of commands needed to work with deferred mode.

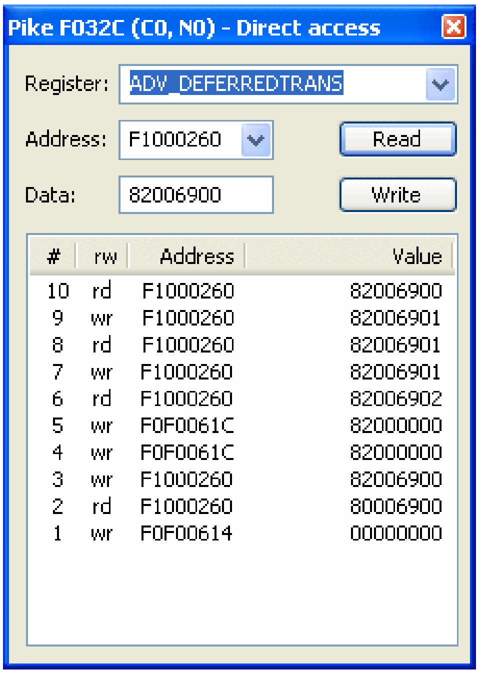


Figure 73: Example: Controlling deferred mode (SmartView - Direct Access; Pike F-032C)

For a description of the commands see the following table:

#	rw	Address	Value	Description
10	rd	F1000260	82006900h	Check how many images are left in image buffer
9	wr	F1000260	86006901h	Read out the second image of image buffer
8	rd	F1000260	82006901h	Check how many images are left in image buffer
7	wr	F1000260	86006901h	Read out the first image of image buffer
6	rd	F1000260	82006902h	Check that two images are in image buffer
5	wr	F0F0061C	82000000h	Do second one-shot
4	wr	F0F0061C	82000000h	Do first one-shot
3	wr	F1000260	82006900h	Switch deferred mode on
2	rd	F1000260	80006900h	Check pres. of deferred mode and image buffer size (69h → 105 frames)
1	wr	F0F00614	00000000h	Stop continuous mode of camera

Table 63: Example: Controlling deferred mode (SmartView - Direct Access; Pike F-032C)

FastCapture mode

Note This mode can be activated only in Format_7.

By setting **FastCapture** to **false**, the maximum frame rate both for image acquisition and read out is associated with the packet size set in the BYTE_PER_PACKET register. The lower this value is, the lower the attainable frame rate is.

By setting **FastCapture** to **true**, all images are recorded at the highest possible frame rate, i.e. the setting above does not affect the frame rate for the image intake but only the read out. The speed of the image transport over the IEEE1394 bus can be defined via the **BytesPerPacket** register. This mode is ideal for applications where a burst of images need to be recorded at the highest sensor speed but the output can be at a lower frame frequency to save bandwidth.

Similar to the HoldImg mode, captured images will be stored in the internal image buffer, if the transport over the IEEE1394 bus is slower than images are captured.

Color interpolation (Bayer demosaicing)

The color sensors capture the color information via so-called primary color (R-G-B) filters placed over the individual pixels in a **Bayer mosaic** layout. An effective Bayer → RGB color interpolation already takes place in all Pike color version cameras.

In color interpolation a red, green or blue value is determined for each pixel. An Allied Vision proprietary Bayer demosaicing algorithm is used for this interpolation (maximum 3x3), optimized for both sharpness of contours as well as reduction of false edge coloring.

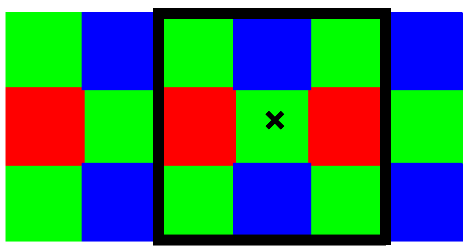


Figure 74: Bayer demosaicing (example of 3x3 matrix)

Color processing can be bypassed by using so-called RAW image transfer.

RAW mode is primarily used to

- save bandwidths on the IEEE1394 bus
- achieve higher frame rates
- use different Bayer demosaicing algorithms on the PC (for Pike F-145 and Pike F-505 the first pixel of the sensor is RED, for all other Pike the first pixel is GREEN followed by RED).

Note

If the PC does not perform Bayer to RGB post-processing, the monochrome image will be superimposed with a checkerboard pattern.

Sharpness

The Pike color models are equipped with a two step sharpness control, applying a discreet horizontal high pass in the Y channel as shown in the next three line profiles.

Sharpness 0, 1 and 2 is calculated with the following scheme:

Sharpness value			
0	0	1	0
1	-0.25	+1.5	-0.25
2	-0.5	2	-0.5

Table 64: Sharpness scheme

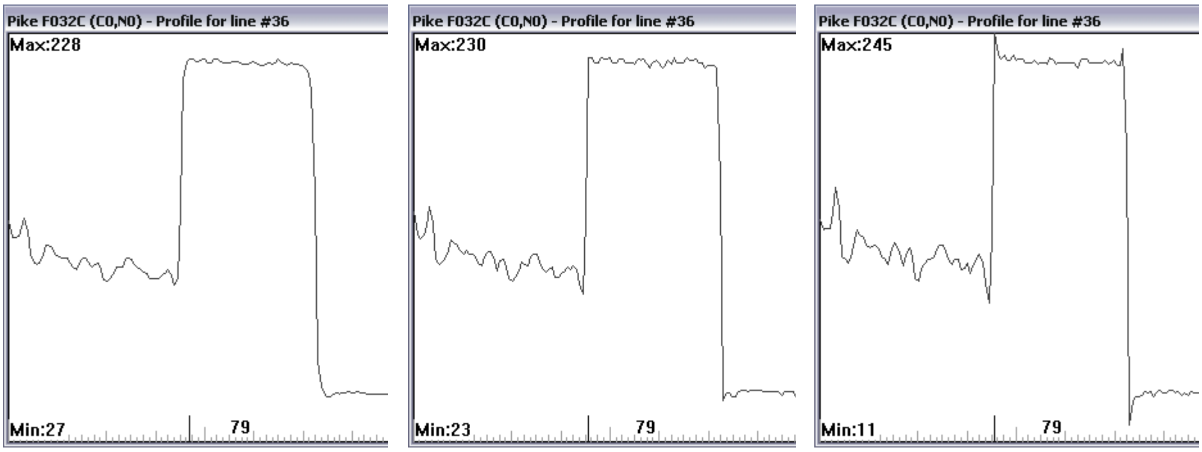


Figure 75: Sharpness: left: 0, middle: 1, right: 2

Note

Sharpness does not show any effect on Pike color models in the Raw8 and Raw16 format, because color processing is put off in all Raw formats.

Note

Configuration

To configure this feature in feature control register, see Table 150: Feature control register on page 282.

Hue and saturation

Pike CCD color models are equipped with **hue** and **saturation** registers.

The **hue register** at offset 810h allows the color of objects to be changed without altering the white balance, by +/- 40 steps (+/- 10°) from the nominal perception. Use this setting to manipulate the color appearance after having carried out the white balance.

The **saturation register** at offset 814h allows the intensity of the colors to be changed between 0 and 200% in steps of 1/256.

This means a setting of zero changes the image to black and white and a setting of 511 doubles the color intensity compared to the nominal one at 256.

Note

Configuration

To configure this feature in feature control register, see Table 150: Feature control register on page 282.

Note

Hue and saturation do not show any effect on Pike color models in the Raw8 and Raw16 format, because color processing is switched off in all Raw formats.

Color correction

Why color correction?

The spectral response of a CCD is different of those of an output device or the human eye. This is the reason for the fact that perfect color reproduction is not possible. In each Pike camera there is a factory setting for the color correction coefficients, see GretagMacbeth ColorChecker on page 167.

Color correction is needed to eliminate the overlap in the color channels. This overlap is caused by the fact that:

- Blue light: is seen by the red and green pixels on the CCD
- Red light: is seen by the blue and green pixels on the CCD
- Green light: is seen by the red and blue pixels on the CCD

The color correction matrix subtracts out this overlap.

Color correction in Allied Vision cameras

In Allied Vision cameras the color correction is realized as an additional step in the process from the sensor data to color output.

Color correction is used to harmonize colors for the human eye. With other Allied Vision (color) cameras so far, you had the opportunity to use it or to switch it off.

Pike cameras introduce for the first time the so-called color correction matrix. This means: you are now able to manipulate the color-correction coefficients yourself.

Color correction: formula

Before converting to the YUV format, color correction on all color models is carried out after Bayer demosaicing via a matrix as follows:

$$\begin{aligned} red^* &= Crr \times red + Cgr \times green + Cbr \times blue \\ green^* &= Crg \times red + Cgg \times green + Cbg \times blue \\ blue^* &= Crb \times red + Cgb \times green + Cbb \times blue \end{aligned}$$

Formula 4: Color correction

GretagMacbeth ColorChecker

Sensor-specific coefficients C_{xy} are scientifically generated to ensure that GretagMacbeth™ ColorChecker®-colors are displayed with highest color fidelity and color balance.

These coefficients are stored in user set 0 and can not be overwritten (factory setting).

Changing color correction coefficients

You can change the color-correction coefficients according to your own needs. Changes are stored in the user settings.

Note

- A number of 1000 equals a color correction coefficient of 1.
- To obtain an identity matrix set values of 1000 for the diagonal elements an 0 for all others. As a result you get colors like in the RAW modes.
- The sums of all rows should be equal to each other. If not, you get tinted images.
- Color correction values range-1000 to +2000 and are signed 32 bit.
- In order for white balance to work properly ensure that the row sum equals 1000.
- Each row should sum up to 1000. If not, images are less or more colorful.
- The maximum row sum is limited to 2000.

Note

Configuration

To configure the color-correction coefficients in an advanced register, see Table 172: Advanced register: Color correction on page 311.

To change the color-correction coefficients in **SmartView**, go to **Adv3** tab.

Switch color correction on/off

Color correction can also be switched off in YUV mode:

Note

Configuration

To configure this feature in an advanced register, see Table 172: Advanced register: Color correction on page 311.

Note

Color correction is deactivated in RAW mode.

Color conversion (RGB → YUV)

The conversion from RGB to YUV is made using the following formulae:

$$
\begin{aligned}
Y &= 0.3 \times R + 0.59 \times G + 0.11 \times B \\
U &= -0.169 \times R - 0.33 \times G + 0.498 \times B + 128 \text{ (@ 8 bit)} \\
V &= 0.498 \times R - 0.420 \times G - 0.082 \times B + 128 \text{ (@ 8 bit)}
\end{aligned}
$$

Formula 5: RGB to YUV conversion

Note

- As mentioned above: Color processing can be bypassed by using so-called RAW image transfer.
- RGB → YUV conversion can be bypassed by using RGB8 format and mode. This is advantageous for edge color definition but needs more bandwidth (300% instead of 200% relative to monochrome or RAW consumption) for the transmission, so that the maximum frame frequency will drop.

Bulk Trigger

See Trigger modes on page 174 and the following pages.

Level Trigger

See Trigger Mode 1 in Trigger modes on page 174.

Serial interface

All Pike cameras are equipped with the SIO (serial input/output) feature as described in IIDC V1.31. This means that the Pike's serial interface can be used as a general RS232 interface.

Data written to a specific address in the IEEE1394 address range will be sent through the serial interface. Incoming data of the serial interface is put in a camera buffer and can be polled via simple read commands from this buffer. Controlling registers enable the settings of baud rates and the check of buffer sizes and serial interface errors.

Note

- Hardware handshaking is not supported.
- Typical PC hardware does not usually support 230400 bps or more.

Base address for the function is: F0F02100h.

To configure this feature in access control register (CSR):

Offset	Name	Field	Bit	Description
000h	SERIAL_MODE_REG	Baud_Rate	[0 to 7]	Baud rate setting WR: Set baud rate RD: Read baud rate 0: 300 bps 1: 600 bps 2: 1200 bps 3: 2400 bps 4: 4800 bps 5: 9600 bps 6: 19200 bps 7: 38400 bps 8: 57600 bps 9: 115200 bps 10: 230400 bps Other values reserved
		Char_Length	[8 to 15]	Character length setting WR: Set data length (7 or 8 bit) RD: Get data length 7: 7 bits 8: 8 bits Other values reserved
		Parity	[16 to 17]	Parity setting WR: Set parity RD: Get parity setting 0: None 1: Odd 2: Even
		Stop_Bit	[18 to 19]	Stop bits WR: Set stop bit RD: Get stop bit setting 0: 1 1: 1.5 2: 2
		---	[20 to 23]	Reserved
		Buffer_Size_Inq	[24 to 31]	Buffer Size (RD only) This field indicates the maximum size of receive/transmit data buffer. If this value=1, Buffer_Status_Control and SIO_Data_Register Char 1-3 should be ignored.

Table 65: Serial input/output control and status register (SIO CSR)

Offset	Name	Field	Bit	Description
0004h	SERIAL_CONTROL_REG	RE	[0]	Receive enable RD: Current status WR: 0: Disable 1: Enable
		TE	[1]	Transmit enable RD: Current status WR: 0: disable 1: Enable
		---	[2 to 7]	Reserved
	SERIAL_STATUS_REG	TDRD	[8]	Transmit data buffer ready Read only 0: not ready 1: ready
		---	[9]	Reserved
		RDRD	[10]	Receive data buffer ready Read only 0: not ready 1: ready
		---	[11]	Reserved
		ORER	[12]	Receive data buffer overrun error Read: current status WR: 0: no error (to clear status) 1: Ignored
		FER	[13]	Receive data framing error Read: current status WR: 0: no error (to clear status) 1: Ignored
		PER	[14]	Receive data parity error Read: current status WR: 0: no error (to clear status) 1: Ignored
		---	[15 to 31]	Reserved

Table 65: Serial input/output control and status register (SIO CSR) (continued)

Offset	Name	Field	Bit	Description
008h	RECEIVE_BUFFER_ STATUS_CONTRL	RBUF_ST	[0 to 7]	SIO receive buffer status RD: Number of bytes pending in receive buffer WR: Ignored
		RBUF_CNT	[8 to 15]	SIO receive buffer control RD: Number of bytes to be read from the receive FiFo WR: Number of bytes left for readout from the receive FiFo
		---	[16 to 31]	Reserved
00Ch	TRANSMIT_BUFFER_ STATUS_CONTRL	TBUF_ST	[0 to 7]	SIO output buffer status RD: Space left in TX buffer WR: Ignored
		TBUF_CNT	[8 to 15]	SIO output buffer control RD: Number of bytes written to transmit FiFo WR: Number of bytes to transmit
		---	[16 to 31]	Reserved
010h .. 0FFh		---		Reserved
100h	SIO_DATA_REGISTER	CHAR_0	[0 to 7]	Character_0 RD: Read character from receive buffer WR: Write character to transmit buffer
	SIO_DATA_REGISTER	CHAR_1	[8 to 15]	Character_1 RD: Read character from receive buffer+1 WR: Write character to transmit buffer+1
	SIO_DATA_REGISTER	CHAR_2	[16 to 23]	Character_2 RD: Read character from receive buffer+2 WR: Write character to transmit buffer+2
	SIO_DATA_REGISTER	CHAR_3	[24 to 31]	Character_3 RD: Read character from receive buffer+3 WR: Write character to transmit buffer+3
104h .. 1FFH	SIO_DATA_REGISTER_A LIAS		[0 to 31]	Alias SIO_Data_Register area for block transfer

Table 65: Serial input/output control and status register (SIO CSR) (continued)

To read data:

1. Query RDRD flag (buffer ready?) and write the number of bytes the host wants to read to RBUF_CNT.
2. Read the number of bytes pending in the receive buffer RBUF_ST (more data in the buffer than the host wanted to read?) and the number of bytes left for reading from the receive FiFo in RBUF_CNT (host wanted to read more data than were in the buffer?).
3. Read received characters from SIO_DATA_REGISTER, beginning at char 0.
4. To input more characters, repeat from step 1.

To write data:

1. Query TDRD flag (buffer ready?) and write the number of bytes to send (copied from SIO register to transmit FiFo) to TBUF_CNT.
2. Read the available data space left in TBUF_ST (if the buffer can hold more bytes than are to be transmitted) and number of bytes written to transmit buffer in TBUF_CNT (if more data is to be transmitted than fits in the buffer).
3. Write character to SIO_DATA_REGISTER, beginning at char 0.
4. To output more characters, repeat from step 1.

Note

- Contact your local distribution partner if you require further information or additional test programs or software.
- Allied Vision recommends the use of Hyperterminal™ or other communication programs to test the functionality of this feature. Alternatively use SmartView to try out this feature.

Controlling image capture

Shutter modes The cameras support the SHUTTER_MODES specified in IIDC V1.31. For all models this shutter is a global pipelined shutter; meaning that all pixels are exposed to the light at the same moment and for the same time span.

Pipelined Pipelined means that the shutter for a new image can already happen, while the preceding image is transmitted.

Continuous mode In continuous modes the shutter is opened shortly before the vertical reset happens, thus acting in a frame-synchronous way.

External trigger Combined with an external trigger, it becomes asynchronous in the sense that it occurs whenever the external trigger occurs. Individual images are recorded when an external trigger impulse is present. This ensures that even fast moving objects can be grabbed with no image lag and with minimal image blur.

Camera I/O The external trigger is fed as a TTL signal through Pin 4 of the camera I/O connector.

Trigger modes

Pike cameras support IIDC conforming Trigger_Mode_0 and Trigger_Mode_1 and special Trigger_Mode_15 (bulk trigger).

Trigger Mode	also known as	Description
Trigger_Mode_0	Edge mode	Sets the shutter time according to the value set in the shutter (or extended shutter) register
Trigger_Mode_1	Level mode	Sets the shutter time according to the active low time of the pulse applied (or active high time in the case of an inverting input)
Trigger_Mode_15	Programmable mode	Is a bulk trigger, combining one external trigger event with continuous or one-shot or multi-shot internal trigger

Table 66: Trigger modes

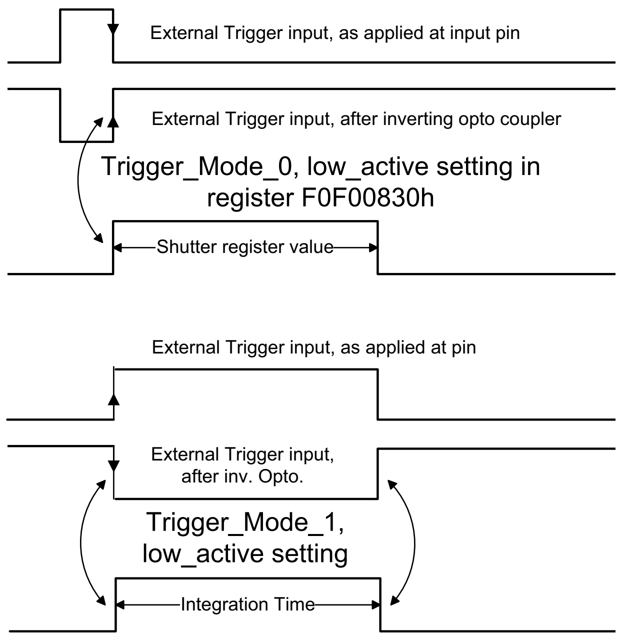


Figure 76: Trigger_Mode_0 and 1

Bulk Trigger (Trigger_Mode_15)

Trigger_Mode_15 is an extension to the IIDC trigger modes. One external trigger event can be used to trigger a multitude of internal image intakes.

This is especially useful for:

- Grabbing exactly one image based on the first external trigger.
- Filling the camera's internal image buffer with one external trigger without overriding images.
- Grabbing an unlimited amount of images after one external trigger (surveillance)

The Figure below illustrates this mode.

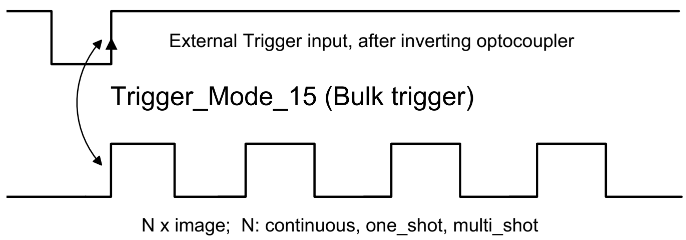


Figure 77: Trigger_Mode_15 (bulk trigger)

The functionality is controlled via bit [6] and bitgroup [12 to 15] of the following register.

Register	Name	Field	Bit	Description
0xF0F00830	TRIGGER_MODE	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1 the value in the Value field has to be ignored
		---	[2 to 5]	Reserved
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON In this bit = 0, other fields will be read only.
		Trigger_Polarity	[7]	Select trigger polarity (Except for software trigger) If Polarity_Inq is 1: Write to change polarity of the trigger input. Read to get polarity of the trigger input. If Polarity_Inq is 0: Read only. 0: Low active input 1: High active input
		Trigger_Source	[8 to 10]	Select trigger source Set trigger source ID from trigger source ID_Inq
		Trigger_Value	[11]	Trigger input raw signal value read only 0: Low 1: High
		Trigger_Mode	[12 to 15]	Trigger_Mode (Trigger_Mode_0..15)
		---	[16 to 19]	Reserved
		Parameter	[20 to 31]	Parameter for trigger function, if required (optional)

Table 67: Trigger_Mode_15 (Bulk Trigger)

The screenshots below illustrate the use of Trigger_Mode_15 on a register level:

- Line #1 switches continuous mode off, leaving viewer in listen mode.
- Line #2 prepares 830h register for external trigger and Mode_15.

Left = continuous	Middle = one-shot	Right = multi-shot
Line #3 switches camera back to continuous mode. Only one image is grabbed precisely with the first external trigger. To repeat rewrite line three.	Line #3 toggles one-shot bit [0] of the one-shot register 61C so that only one image is grabbed, based on the first external trigger. To repeat rewrite line three.	Line #3 toggles multi-shot bit [1] of the one-shot register 61C so that Ah images are grabbed, starting with the first external trigger. To repeat rewrite line three.

Table 68: Description: using Trigger_Mode_15: continuous, one-shot, multi-shot

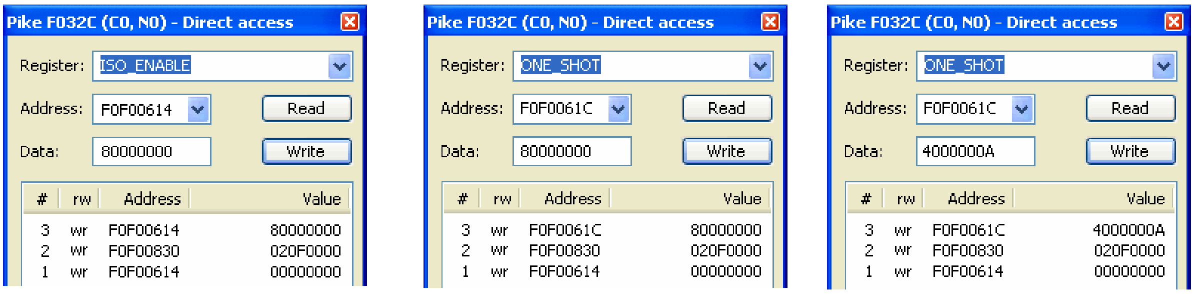


Figure 78: Using Trigger_Mode_15: continuous, one-shot, multi-shot

Note

Shutter for the images is controlled by shutter register.

Trigger delay

As already mentioned earlier the cameras feature various ways to delay image capture based on external trigger.

With IIDC V1.31 there is a standard CSR at Register F0F00534/834h to control a delay up to FFFh × time base value.

The following table explains the Inquiry register and the meaning of the various bits.

Register	Name	Field	Bit	Description
0xF0F00534	TRIGGER_DLY_INQUIRY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Abs_Control_Inq	[1]	Capability of control with absolute value
		---	[2]	Reserved
		One_Push_Inq	[3]	One Push auto mode (controlled automatically by the camera once)
		ReadOut_Inq	[4]	Capability of reading out the value of this feature
		On_Off_Inq	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Auto Mode (controlled automatically by the camera)
		Manual_Inq	[7]	Manual Mode (controlled by user)
		Min_Value	[8 to 19]	Minimum value for this feature
		Max_Value	[20 to 31]	Maximum value for this feature

Table 69: Trigger delay inquiry register

Register	Name	Field	Bit	Description
0xF0F00834	TRIGGER_DELAY	Presence_Inq	[0]	Presence of this feature: 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control O: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, the value in the Value field has to be ignored
		-	[2 to 5]	Reserved
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON In this bit = 0, other fields will be read only.
		-	[7 to 19]	Reserved
		Value	[20 to 31]	Value If you write the value in OFF mode, this field will be ignored. If ReadOut capability is not available, then the read value will have no meaning.

Table 70: CSR: Trigger delay

Trigger delay advanced register

In addition, the cameras have an advanced register which allows even more precise image capture delay after receiving a hardware trigger.

Register	Name	Field	Bit	Description
0xF1000400	TRIGGER_DELAY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	-
		ON_OFF	[6]	Trigger delay on/off
		---	[7 to 10]	-
		DelayTime	[11 to 31]	Delay time in µs

Table 71: Advanced CSR: Trigger delay

The advanced register allows start of the integration to be delayed by maximum 2^{21} µs, which is maximum 2.1 s after a trigger edge was detected.

Note

- Switching trigger delay to ON also switches external Trigger_Mode_0 to ON.
- This feature works with external Trigger_Mode_0 only.

Debounce

Only for input ports:

There is an adjustable debounce time for trigger: separate for each input pin. The debounce time is a waiting period where no new trigger is allowed. This helps you to set exact one trigger.

The debounce feature is applied in cases of bad signals. The aim is to let the trigger run, when the signal is debounced.

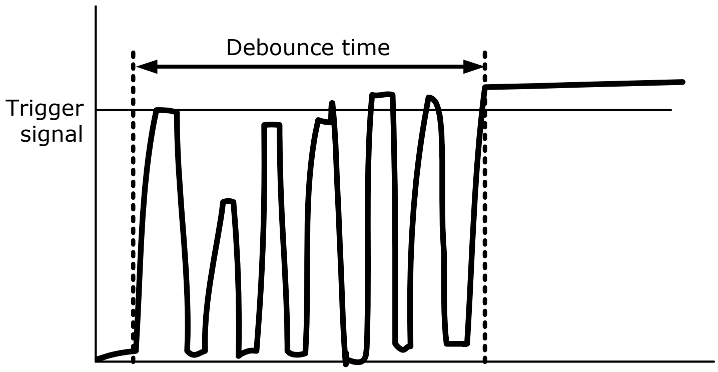


Figure 79: Example of debounce time for trigger

To set this feature in an advanced register, see Debounce time on page 182.

To set this feature in SmartView: Trig/IO tab, Input pins table, Debounce column.

Low pass Debounce acts like a low-pass filter with debounce time acting as resistance-capacitance element. That means: with increasing debounce time trigger will release later.

Example Debounce time set to 20 µs.

A switch debounces with 5 µs high pulse and 1 µs low pulse. During high pulse an internal counter adds one cycle, during low pulse the counter subtracts one cycle. Therefore high pulses at input pin have to be ≥ 20 µs.

Internal counter sees: 5 µs - 1 µs = 4 µs

Number of periods during debounce time: 20 µs / 4 µs = 5
That means 5 periods × 6 µs = 30 µs

The trigger starts after 30 µs while the debounce time was set to 20 µs.

Note

The pulse width (total time of high and low pulses) must be greater than the debounce time.

Debounce time

This register controls the debounce feature of the cameras input pins. The debounce time can be set for each available input separately.

Increment is 500 ns

Debounce time is set in Time × 500 ns

Minimum debounce time is 1.5 µs ⇨ 3 × 500 ns

Maximum debounce time is ~16 ms ⇨ $(2^{15}-1) \times 500$ ns

Offset	Name	Field	Bit	Description
0xF1000840	IO_INP_DEBOUNCE_1	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[2 to 7]	Reserved
		Time	[8 to 31]	Debounce time in steps of 500 ns (24 bit) see examples above
0xF1000844		MinValue	[0 to 31]	Minimum debounce time
0xF1000848		MaxValue	[0 to 31]	Maximum debounce time
0xF100084C		---	[0 to 31]	Reserved
0xF1000850	IO_INP_DEBOUNCE_2			same as IO_INP_DEBOUNCE_1
0xF1000860	IO_INP_DEBOUNCE_3			same as IO_INP_DEBOUNCE_1
0xF1000870	IO_INP_DEBOUNCE_4			same as IO_INP_DEBOUNCE_1
0xF1000880				Reserved
0xF1000890				Reserved
0xF10008A0				Reserved
0xF10008B0				Reserved

Table 72: Advanced register: Debounce time for input ports

Note

- The camera corrects invalid values automatically.
- This feature is not stored in the user settings.

Exposure time (shutter) and offset

The exposure (shutter) time for continuous mode and Trigger_Mode_0 is based on the following formula:

Shutter register value × time base + offset

The register value is the value set in the corresponding IIDC 1.31 register (SHUTTER [81Ch]). This number is in the range between 1 and 4095.

The shutter register value is multiplied by the time base register value (see Table 160: Time base ID on page 297). The default value here is set to 20 µs.

A camera-specific offset is also added to this value. It is different for the camera models:

Exposure time offset

Camera model	Exposure time offset
Pike F-032	17 µs
Pike F-100	42 µs
Pike F-145	38 µs
Pike F-145-15fps	70 µs
Pike F-210	42 µs
Pike F-421	69 µs
Pike F-505	26 µs
Pike F-1100	128 µs
Pike F-1600	635 µs

Table 73: Camera-specific exposure time offset

Minimum exposure time

Model	Minimum exposure time	Effective min. exp. time = Min. exp. time + offset
Pike F-032	1 µs	1 µs + 17 µs = 18 µs
Pike F-100	1 µs	1 µs + 42 µs = 43 µs
Pike F-145	1 µs	1 µs + 38 µs = 39 µs
Pike F-145-15fps	1 µs	1 µs + 70 µs = 71 µs
Pike F-210	1 µs	1 µs + 42 µs = 43 µs
Pike F-421	1 µs	1 µs + 69 µs = 70 µs

Table 74: Camera-specific minimum exposure time

Model	Minimum exposure time	Effective min. exp. time = Min. exp. time + offset
Pike F-505	1 µs	1 µs + 26 µs = 27 µs
Pike F-1100	1 µs	1 µs + 128 µs = 129 µs
Pike F-1600	1 µs	1 µs + 635 µs = 636 µs

Table 74: Camera-specific minimum exposure time (continued)

Example: Pike F-032

Camera	Register value	Time base (default)
Pike F-032	100	20 µs

Table 75: Register value and time base for Pike F-032

register value × time base = exposure time

100 × 20 µs + 17 µs = 2017 µs exposure time

The minimum adjustable exposure time set by register is 1 µs. → The real minimum exposure time of Pike F-032 is then:
1 µs + 17 µs = 18 µs

Extended shutter

The exposure time for long-term integration of up to 67 seconds can be extended via the advanced register: EXTENDED_SHUTTER

Register	Name	Field	Bit	Description
0xF100020C	EXTD_SHUTTER	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	
		ExpTime	[6 to 31]	Exposure time in µs

Table 76: Advanced register: Extended shutter

The longest exposure time, 3FFFFFFh, corresponds to 67.11 sec.

The lowest possible value of ExpTime is camera-specific, see Table 74: Camera-specific minimum exposure time on page 183.

Note

- Exposure times entered via the 81Ch register are mirrored in the extended register, but not vice versa.
- Longer integration times not only increase sensitivity, but may also increase some unwanted effects such as noise and pixel-to-pixel non-uniformity. Depending on the application, these effects may limit the longest usable integration time.
- Changes in this register have immediate effect, even when the camera is transmitting.
- Extended shutter becomes inactive after writing to a format/mode/frame rate register.

One-shot

The camera can record an image by setting the one-shot bit in the 61Ch register. This bit is automatically cleared after the image is captured. If the camera is placed in ISO_Enable mode, see ISO_Enable / free-run on page 188, this flag is ignored.

If one-shot mode is combined with the external trigger, the one-shot command is used to arm it. The following screenshot shows the sequence of commands needed to put the camera into this mode. It enables the camera to grab exactly one image with an external trigger edge.

If there is no trigger impulse after the camera has been armed, one-shot can be canceled by clearing the bit.

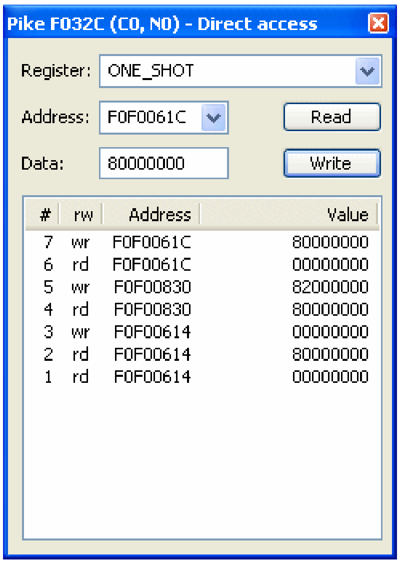


Figure 80: One-shot control (SmartView)

#	Read = rd Write = wr	Address	Value	Description
7	wr	F0F0061C	80000000	Do one-shot.
6	rd	F0F0061C	00000000	Read out one-shot register.
5	wr	F0F00830	82000000	Switch on external trigger mode 0.
4	rd	F0F00830	80000000	Check trigger status.
3	wr	F0F00614	00000000	Stop free-run.
2	rd	F0F00614	80000000	Check Iso_Enable mode (→free-run).
1	rd	F0F00614	00000000	This line is produced by SmartView.

Table 77: One-shot control: descriptions

One-shot command on the bus to start of exposure

The following sections describe the time response of the camera using a single frame (one-shot) command. As set out in the IIDC specification, this is a software command that causes the camera to record and transmit a single frame.

The following values apply only when the camera is idle and ready for use. Full resolution must also be set.

Feature	Value
One-shot → microcontroller sync	≤ 150 µs (processing time in the microcontroller)
µC-Sync/ExSync → integration start	8 µs

Table 78: Values for one-shot

Microcontroller sync is an internal signal. It is generated by the microcontroller to initiate a trigger. This can either be a direct trigger or a release for ExSync if the camera is externally triggered.

End of exposure to first packet on the bus

After the exposure, the CCD sensor is read out; some data is written into the FRAME_BUFFER before being transmitted to the bus.

The time from the end of exposure to the start of transport on the bus is:

710 µs ± 62.5 µs

This time *jitters* with the cycle time of the bus (125 µs).

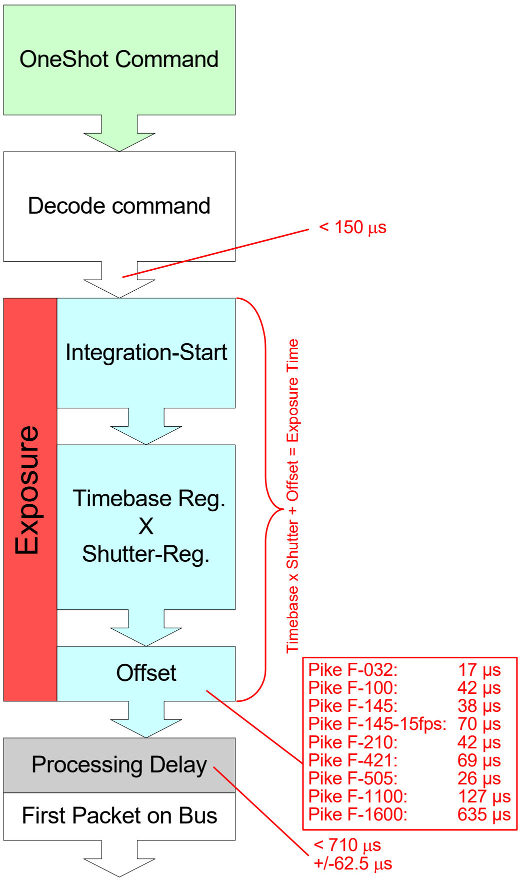


Figure 81: Data flow and timing after end of exposure

Multi-shot

Setting multi-shot and entering a quantity of images in Count_Number in the 61Ch register enables the camera to record a specified number of images.

The number is indicated in bits 16 to 31. If the camera is put into ISO_Enable mode (see ISO_Enable / free-run on page 188), this flag is ignored and deleted automatically once all the images have been recorded.

If multi-shot mode is activated and the images have not yet all been captured, it can be canceled by resetting the flag. The same result can be achieved by setting the number of images to 0.

Multi-shot can also be combined with the external trigger in order to grab a certain number of images based on an external trigger. This is especially helpful in combination with the so called deferred mode to limit the number of grabbed images to the FIFO size.

ISO_Enable / free-run

Setting the MSB (bit 0) in the 614h register (ISO_ENA) puts the camera into ISO_Enable mode or Continuous_Shot (free-run). The camera captures an infinite series of images. This operation can be quit by deleting the 0 bit.

Asynchronous broadcast

The camera accepts asynchronous broadcasts. This involves asynchronous write requests that use node number 63 as the target node with no acknowledge.

This makes it possible for all cameras on a bus to be triggered by software simultaneously - e.g. by broadcasting a one-shot. All cameras receive the one-shot command in the same IEEE1394 bus cycle. This creates uncertainty for all cameras in the range of 125 µs.

Inter-camera latency is described in Jitter at start of exposure on page 189.

The following screenshot shows an example of broadcast commands sent with the Firedemo example of FirePackage:

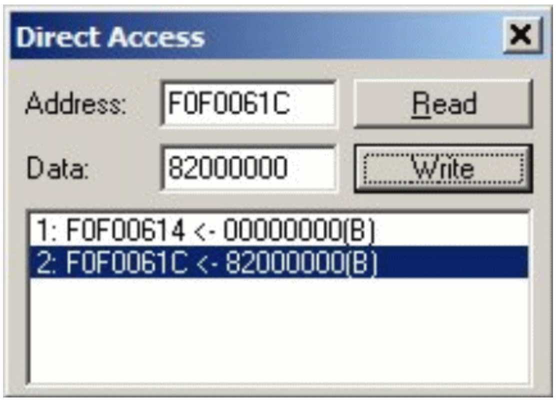


Figure 82: Broadcast one-shot

- Line 1 shows the broadcast command, which stops all cameras connected to the same IEEE1394 bus. It is generated by holding the <shift> key down while clicking on <Write>.
- Line 2 generates a broadcast one_shot in the same way, which forces all connected cameras to simultaneously grab one image.

Jitter at start of exposure

The following chapter discusses the latency time which exists for all Pike CCD models when either a hardware or software trigger is generated, until the actual image exposure starts.

Owing to the well-known fact that an Interline Transfer CCD sensor has both a light sensitive area and a separate storage area, it is common to interleave image exposure of a new frame and output that of the previous one. It makes continuous image flow possible, even with an external trigger.

The uncertain time delay before the start of exposure depends on the state of the sensor. A distinction is made as follows:

FVal is active → the sensor is reading out, the camera is busy

In this case the camera must not change horizontal timing so that the trigger event is synchronized with the current horizontal clock. This introduces a maximum uncertainty which is equivalent to the line time. The line time depends on the sensor used and therefore can vary from model to model.

FVal is inactive → the sensor is ready, the camera is idle

In this case the camera can resynchronize the horizontal clock to the new trigger event, leaving only a very short uncertainty time of the master clock period.

Model	Exposure start jitter (while FVal)	Exposure start jitter (while camera idle)
Pike F-032	± 4.9 µs	± 375 ns
Pike F-100	± 8.2 µs	± 1.65 µs
Pike F-145	± 16 µs	± 2.9 µs
Pike F-145-15fps	± 30 µs	± 5.4 µs
Pike F-210	± 14.25 µs	± 1.8 µs
Pike F-421	± 15 µs	± 1.65 µs
Pike F-505	± 17 µs	± 5.7 µs
Pike F-1100	single tap:± 141 µs dual tap: ± 74.5 µs	± 7.64 µs (single+dual tap)
Pike F-1600	single tap:± 177 µs dual tap: ± 95.7 µs	± 13.6 µs (single+dual tap)

Table 79: Jitter at exposure start (no binning, no sub-sampling)

Note

- Jitter at the beginning of an exposure has no effect on the length of exposure, i.e. it is always constant.

Sequence mode

Generally all Pike cameras enable certain image settings to be modified on the fly, e.g. gain and shutter can be changed by the host computer by writing into the gain and shutter register even while the camera is running. An uncertainty of up to 3 images remains because normally the host does not know (especially with external trigger) when the next image will arrive.

Sequence mode is a different concept where the camera holds a set of different image parameters for a sequence of images. The parameter set is stored volatile in the camera for each image to be recorded. This sequence of parameter sets is simply called a sequence. The advantage is that the camera can easily synchronize this parameter set with the images so that no uncertainty can occur. All Pike cameras support 32 different sequence parameters.

Additionally to the sequence mode known from Marlin cameras, the Pike cameras have:

- Repeat counter per sequence item
- Incrementing list pointer on input status (on/off)
- Pointer reset (software command; on input pin)

Examples

For a sequence of images, each image can be recorded with a different shutter or gain to obtain different brightness effects.

The image area (AOI) of a sequence of images can automatically be modified, thus creating a panning or sequential split screen effect.

The following registers can be modified to affect the individual steps of the sequence. Different configurations can be accessed via e.g a foot switch which is connected to an input.

Mode	These registers can be modified...
All modes	Cur_V_Mode, Cur_V_Format, ISO_Channel, ISO_Speed, Brightness, White_Balance (color models only), Shutter, Gain, LUT, TestImage, Image-Mirror, HSNR, Output-Ctrl, ColorCorrection matrix (color models only), ISO-Channel, Shading-Ctrl, Sequence-Stepping Mode, SIS_UserValue
Fixed modes only	Cur_V_Frm_Rate
Format_7 only	Image_Position (AOI-Top, AOI-Left), Image_Size (AOI-Width, AOI-Height), Color_Coding_ID*, Binning*, Sub-Sampling*, Byte_Per_Packet *hidden in video formats and video modes

Table 80: Registers to be modified within a sequence

Note

Sequence mode requires not only firmware 3.× but also special care if changing image size, Color_Coding_ID and frame rate related parameters. This is because these changes not only affect settings in the camera but also require corresponding settings in the receiving software in the PC.

Caution

Incorrect handling may lead to image corruption or loss of subsequent images.

Please ask for detailed support when you want to use this feature.

How is sequence mode implemented?

There is a FIFO (first in first out) memory for each of the IIDC V1.31 registers listed above. The depth of each FIFO is fixed to 32(dez) complete sets. Functionality is controlled by the following advanced registers.

Register	Name	Field	Bit	Description
0xF1000220	SEQUENCE_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 4]	Reserved
		AutoRewind	[5]	
		ON_OFF	[6]	Enable/disable this feature
		SetupMode	[7]	Sequence setup mode
		---	[8 to 15]	Reserved
		MaxLength	[16 to 23]	Maximum possible length of a sequence (read only)
		SeqLength	[24 to 31]	Length of the sequence (32 dez for all CCD models)
0xF1000224	SEQUENCE_PARAM	---	[0 to 4]	Reserved
		ApplyParameters	[5]	Apply settings to selected image of sequence; auto-reset
		---	[6 to 7]	Reserved
		SeqStepMode	[8 to 15]	Sequence stepping mode
		ImageRepeat	[16 to 23]	Image repeat counter
		ImageNo	[24 to 31]	Number of image within a sequence

Table 81: Advanced register: Sequence mode

Register	Name	Field	Bit	Description
0xF1000228	SEQUENCE_STEP	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 4]	Reserved
		PerformStep	[5]	Sequence is stepped one item forward
		PerformReset	[6]	Reset the sequence to start position
		---	[7 to 23]	Reserved
		SeqPosition	[24 to 31]	Get the current sequence position

Table 81: Advanced register: Sequence mode (continued)

Enabling this feature turns the camera into a special mode. This mode can be used to set up a bunch of parameter sets for up to MaxLength consecutive images.

Note

The sequence mode of the Pike 3.× series firmware behaves slightly different than the sequence mode of e.g. the Marlin series and implements some new controlling features. You may use a sequence with internal or external trigger and with the Deferred Transport feature.

Setup mode (new for 3.×)

The SetupMode flag allows you to set up a sequence while capturing images. Using this flag you get a visual feedback of the settings.

Set SetupMode flag when setting up the sequence and reset the flag before using the sequence.

Sequence step mode (new for 3.×)

The SeqMode field selects the signal source for stepping the sequence one parameter set further.

SeqMode description

Sequence mode	Description
0x80	This mode is the default sequence mode and stepping the sequence is compatible to e.g. the Marlin series. With each image integration start the sequence is stepped one item further and the new parameter set becomes active for the next image.
0x82	Stepping of the sequence is controlled by a rising edge of an external signal. The new parameter set becomes active with the next integration start. When using this mode select the suitable input mode of the input lines.
0x84	Stepping of the sequence is controlled by a high level of an external signal. The new parameter set becomes active with the next integration start. When using this mode select the suitable input mode of the input lines.
Other mode	Choosing any other mode value, automatically defaults to mode 0x80.

Table 82: Sequence mode description

Note

It is also possible, that a sequence consists of parameter sets with different sequence modes. This can be achieved by using the SeqMode and the ImageNo fields within the Sequence_Param register.

Sequence repeat counter (new for 3.×)

For each parameter set one can define an image repeat counter. Using the image repeat counter means that a parameter set can be used for n consecutive images before the next parameter set is applied.

Setting the ImageRepeat field to 0 has the same effect like setting this field to 1.

Manual stepping & reset (new for 3.×)

With firmware 3.× a sequence can be stepped further with a software command. To use manual stepping use stepping mode 0x82 or 0x84, but do not setup any input pin for external sequence stepping.

Every time the PerformStep flag is set the sequence will be stepped one parameter set further. Manual stepping observes the repeat counter also.

For some application it could be useful to reset the sequence during runtime. Simply set the PerformReset flag to one: the sequence starts over with the very first parameter set.

The following flow diagram shows how to set up a sequence.

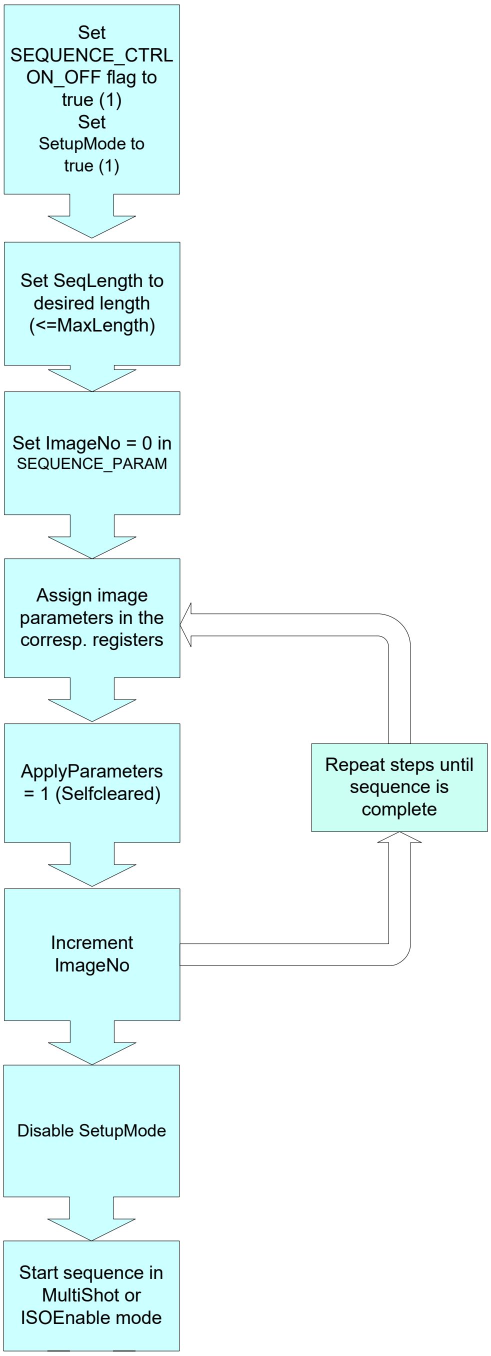


Figure 83: Sequence mode flow diagram

During sequencing, the camera obtains the required parameters, image by image, from the corresponding FIFOs (e.g. information for exposure time).

Which new sequence mode features are available?

New features:

- Repeat one step of a sequence n times where n can be set by the variable ImageRepeat in SEQUENCE_PARAM.
- Define one or two hardware inputs in Input mode field of IO_INP_CTRL as:
  - Sequence step input (if two are set as input, they are AND gated) or
  - Sequence reset input

Note

From now on:

sequence step is I/O controlled sequence stepping mode

sequence reset is I/O controlled sequence pointer reset

Setup mode

The SetupMode flag allows you to set up a sequence while capturing images. Using this flag you get a visual feedback of the settings. Set this flag when setting up the sequence and reset the flag before using the sequence.

I/O controlled sequence stepping mode

The I/O controlled sequence stepping mode can be done level controlled or edge controlled:

Level controlled	Edge controlled
• As long as the input is in high state the sequence pointer will be incremented from image to image. • Can be combined with Quick Format Change Modes. See Standard Parameter Update Timing on page 154 and New: Quick Format Change Mode (QFCM) on page 154. • Level change is asynchronous to image change.	• A rising edge on the input will cause one pointer increment immediately. • Can be combined with Quick Format Change Modes. See Standard Parameter Update Timing on page 154 and New: Quick Format Change Mode (QFCM) on page 154.

Table 83: Description of sequence stepping control

The I/O controlled sequence stepping mode can be set for every single sequence entry. Thus a sequence can be controlled in a very flexible manner.

I/O controlled sequence pointer reset

I/O controlled sequence pointer reset is always edge controlled. A rising edge on the input pin resets the pointer to the first entry.

I/O controlled sequence pointer reset can be combined with Quick Format Change Modes. See Standard Parameter Update Timing on page 154 and New: Quick Format Change Mode (QFCM) on page 154.

I/O controlled sequence stepping mode and I/O controlled sequence pointer reset via software command

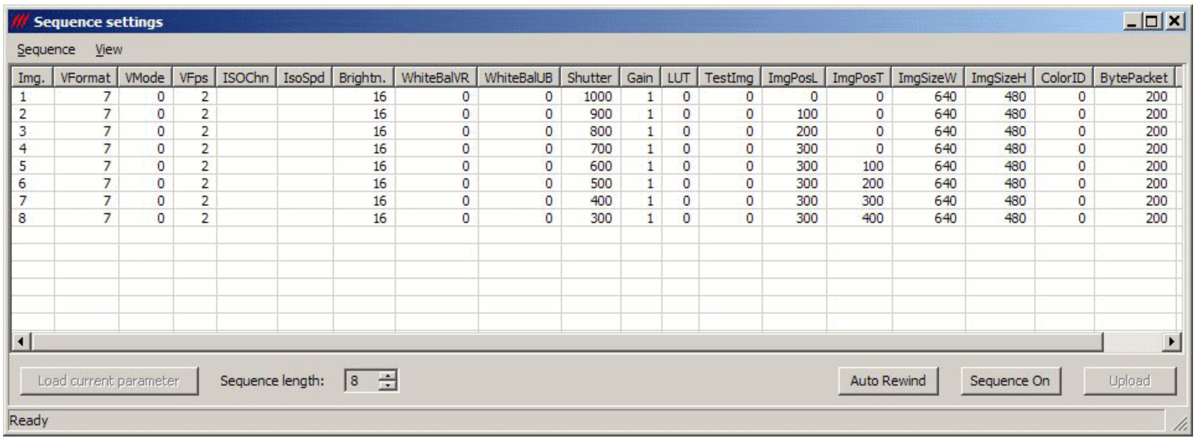
Both sequence modes can be controlled via software command.

Points to pay attention to when working with a sequence

Note

- If more images are recorded than defined in SeqLength, the settings for the last image remain in effect.
- If sequence mode is canceled, the camera can use the FIFO for other tasks. For this reason, a sequence must be loaded back into the camera after sequence mode has been canceled.
- To repeat the sequence, stop the camera and send the multi-shot or IsoEnable command again. Each of these two commands resets the sequence.
- Using SingleShot mode in combination with a sequence does not make sense, because SingleShot mode restarts the sequence every time.
- The sequence may not be active when setting the AutoRewind flag. For this reason it is important to set the flag before the multi-shot or IsoEnable commands.
- If the sequence is used with the deferred transport feature, the number of images entered in Seq_Length may not be exceeded.

The following screenshot shows an example of a sequence for eight different image settings. It uses the Firetool program as graphical representation. Please note the changes in the shutter time; that creates descending image brightness, and the change in the image position; which creates a panning effect.



Sequence settings

Sequence View

Img.	VFormat	VMode	VFps	ISOChn	IsoSpd	Brightn.	WhiteBalVR	WhiteBalUB	Shutter	Gain	LUT	TestImg	ImgPosL	ImgPosT	ImgSizeW	ImgSizeH	ColorID	BytePacket
1	7	0	2			16	0	0	1000	1	0	0	0	0	640	480	0	200
2	7	0	2			16	0	0	900	1	0	0	100	0	640	480	0	200
3	7	0	2			16	0	0	800	1	0	0	200	0	640	480	0	200
4	7	0	2			16	0	0	700	1	0	0	300	0	640	480	0	200
5	7	0	2			16	0	0	600	1	0	0	300	100	640	480	0	200
6	7	0	2			16	0	0	500	1	0	0	300	200	640	480	0	200
7	7	0	2			16	0	0	400	1	0	0	300	300	640	480	0	200
8	7	0	2			16	0	0	300	1	0	0	300	400	640	480	0	200

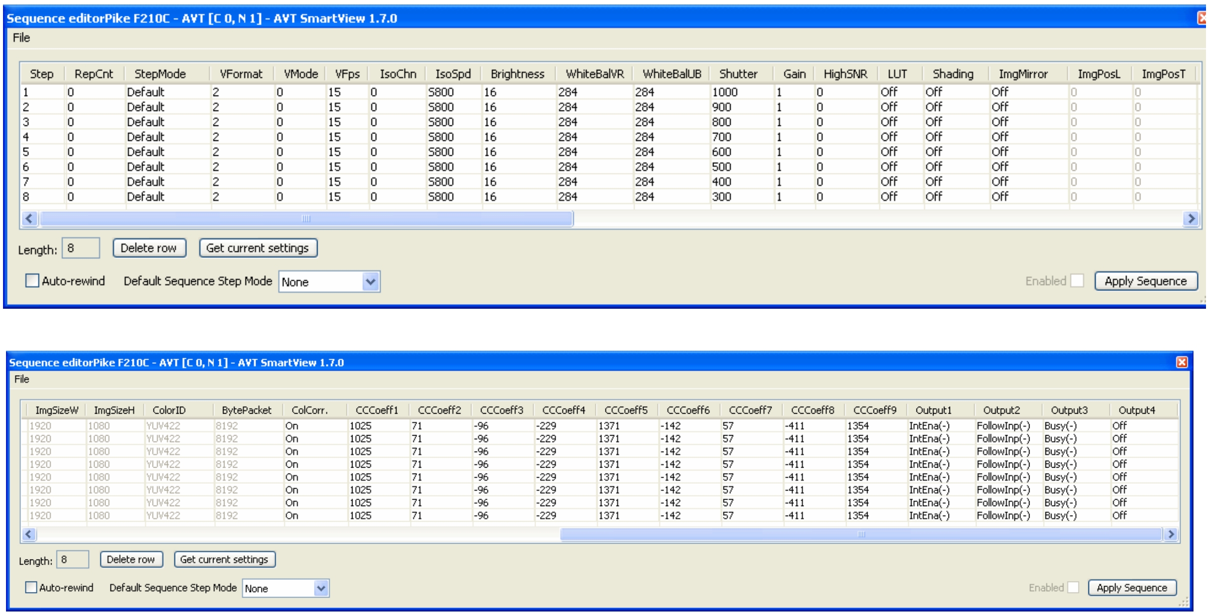
Load current parameter Sequence length: 8 Auto Rewind Sequence On Upload

Ready

Figure 84: Example of sequence mode settings

Instead of Firetool you also can use SmartView (Version 1.7.0 or greater), but image and transfer formats have to be unchanged (height, width, ColorID).

To open the Sequence editor in SmartView: Click Extras → Sequence dialog



Sequence editorPike F210C - AVT [C 0, N 1] - AVT SmartView 1.7.0

File

Step	RepCnt	StepMode	VFormat	VMode	VFps	IsoChn	IsoSpd	Brightness	WhiteBalVR	WhiteBalUB	Shutter	Gain	HighSNR	LUT	Shading	ImgMirror	ImgPosL	ImgPosT
1	0	Default	2	0	15	0	S800	16	284	284	1000	1	0	Off	Off	Off	0	0
2	0	Default	2	0	15	0	S800	16	284	284	900	1	0	Off	Off	Off	0	0
3	0	Default	2	0	15	0	S800	16	284	284	800	1	0	Off	Off	Off	0	0
4	0	Default	2	0	15	0	S800	16	284	284	700	1	0	Off	Off	Off	0	0
5	0	Default	2	0	15	0	S800	16	284	284	600	1	0	Off	Off	Off	0	0
6	0	Default	2	0	15	0	S800	16	284	284	500	1	0	Off	Off	Off	0	0
7	0	Default	2	0	15	0	S800	16	284	284	400	1	0	Off	Off	Off	0	0
8	0	Default	2	0	15	0	S800	16	284	284	300	1	0	Off	Off	Off	0	0

Length: 8 Delete row Get current settings

Auto-rewind Default Sequence Step Mode None Enabled Apply Sequence

Sequence editorPike F210C - AVT [C 0, N 1] - AVT SmartView 1.7.0

File

ImgSizeW	ImgSizeH	ColorID	BytePacket	ColCorr.	CCCoeff1	CCCoeff2	CCCoeff3	CCCoeff4	CCCoeff5	CCCoeff6	CCCoeff7	CCCoeff8	CCCoeff9	Output1	Output2	Output3	Output4
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off
1920	1080	YUV422	8192	On	1025	71	-96	-229	1371	-142	57	-411	1354	IntEna(-)	FollowInp(-)	Busy(-)	Off

Length: 8 Delete row Get current settings

Auto-rewind Default Sequence Step Mode None Enabled Apply Sequence

Figure 85: SmartView: Extras → Sequence dialog

Changing the parameters within a sequence

To change the parameter set for one image, it is not necessary to modify the settings for the entire sequence. The image can simply be selected via the ImageNo field and it is then possible to change the corresponding IIDC V1.31 registers.

Points to pay attention to when changing the parameters

Note

- If the ApplyParameters flag is used when setting the parameters, all not-configured values are set to default values. As changing a sequence normally affects only the value of a specific register, and all other registers should not be changed, the ApplyParameters flag may not be used here.
- The values stored for individual images can no longer be read.
- If the camera is switched into sequence mode, the changes to the IIDC V1.31 registers for the image specified in ImageNo take immediate effect.
- Sequence mode requires firmware 3.× and special care if changing image size and frame rate related parameters. This is because these changes not only affect settings in the camera but also require corresponding settings in the receiving software in the PC (e.g. FirePackage).

Caution

Incorrect handling may lead to image corruption or loss of subsequent images.

Please ask for detailed support when you want to use this feature.

Secure image signature (SIS): definition and scenarios

Note

For all customers who know SIS from Marlin cameras:

- Pike cameras have additional SIS features: AOI, exposure/gain, input/output state, index of sequence mode and serial number.
- In contrary to Marlin cameras, in the Pike SIS feature the endianness cannot be changed.

SIS: Definition

Secure image signature (SIS) is the synonym for data, which is inserted into an image to improve or check image integrity.

With the new firmware 3.x, all Pike models can insert

- Time stamp (IEEE1394 bus cycle time at the beginning of integration)
- Trigger counter (external trigger seen only)
- Frame counter (frames read out of the sensor)
- AOI (x, y, width, height)
- Exposure (shutter) and gain
- Input and output state on exposure start
- Index of sequence mode
- Serial number
- User value

into a selectable line position within the image. Furthermore the trigger counter and the frame counter are available as advanced registers to be read out directly.

SIS: Scenarios

The following scenarios benefit from this feature:

- Assuming camera runs in continuous mode, the check of monotonically changing bus cycle time is a simple test that no image was skipped or lost in the camera or subsequently in the image processing chain.
- In (synchronized) multi camera applications, the time stamp can be used to identify those images, shot at the same moment in time.
- The cross-check of the frame counter of the camera against the frame counter of the host system also identifies any skipped or lost images during transmission.
- The cross-check of the trigger counter against the frame counter in the camera can identify a trigger overrun in the camera.
- AOI can be inserted in the image if it was set as a variable e.g. in a sequence.
- Exposure/gain scenario parameters can be inserted in the image if set as a variable in e.g. sequence mode to identify the imaging conditions.
- Inserting input and output state on exposure start can be helpful when working with input and output signals.
- Index of sequence mode can be inserted if SIS is used together with sequence mode.
- Serial number inserted in the image helps to document/identify the camera in e.g. multi camera applications.

Note

FirePackage offers additional and independent checks to be performed for the purpose of image integrity. Details can be found in the respective documentation.

Note

More information:

The handling of the SIS feature is fully described in the Secure image signature (SIS) on page 323.

Smear reduction (not Pike F-1100, F-1600)

Smear reduction: definition

Definition Smear is an undesirable CCD sensor artifact creating a vertical bright line that extends above and below a bright spot in an image.

Definition Smear reduction is a function implemented in hardware in the camera itself to compensate for smear.

Smear reduction: how it works

To reduce smear a reference line is used. This reference line is built from the mean value of the so-called black lines (two lines before image start). The reference line is subtracted from every line of the whole image.

But how will this reduce smearing?

The point is: black lines have no image information but are also affected from smearing. Thus the smearing effect itself is isolated and can be reduced in the whole image.

The two additional black lines and the calculated anti-smear values do not lower the transfer rates significantly due to hardware implementation.

Smear reduction: switch on/off in register and SmartView

To switch on/off smear reduction in advanced registers, see Smear reduction (not Pike F-1100, F-1600) on page 328.

In SmartView: Edit settings → Adv3 tab (Smear reduction ☑ Enable)

Video formats, modes and bandwidth

The different Pike models support different video formats, modes and frame rates.

These formats and modes are standardized in the IIDC (formerly DCAM) specification.

Resolutions smaller than the generic sensor resolution are generated from the center of the sensor and without binning.

Note

- The maximum frame rates can only be achieved with shutter settings lower than 1/framerate. This means that with default shutter time of 40 ms, a camera will not achieve frame rates higher than 25 frames/s. In order to achieve higher frame rates, please reduce the shutter time proportionally.
- The following tables assume that bus speed is 800 Mbit/s. With lower bus speeds (e.g. 400, 200 or 100 Mbit/s) not all frame rates may be achieved.
- For information on bit/pixel and byte/pixel for each color mode see Table 132: ByteDepth on page 254.

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Note

H-binning means horizontal binning.

V-binning means vertical binning.

Full binning (H+V) means horizontal + vertical binning

2 × binning means: 2 neighboring pixels are combined.

4 × binning means: 4 neighboring pixels are combined.

- Binning average means: signals form adjacent pixels are combined by averaging.
- Binning increases signal-to-noise ratio (SNR), but decreases resolution.

Pike F-032B, F-032C

Format	Mode	Resolution	Color mode	120 fps	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444							
	1	320 × 240	YUV422	✔	✔	✔	✔	✔	✔	✔
	2	640 × 480	YUV411	✔	✔	✔	✔	✔	✔	✔
	3	640 × 480	YUV422		✔	✔	✔	✔	✔	✔
	4	640 × 480	RGB8		✔	✔	✔	✔	✔	✔
	5	640 × 480	Mono8	✔ ✔	✔ ✔	✔ ✔	✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	640 × 480	Mono16		✔	✔	✔	✔	✔	✔

Table 84: Video fixed format for Pike F-032B, Pike F-032C

Frame rates with shading are only achievable with IEEE1394b (S800).

Note

The following Format_7 table shows default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	640 × 480 640 × 480	Mono8 Mono12 Mono16 YUV411,Raw12 YUV422,Raw16 Mono8,Raw8 RGB8	208 fps 139 fps 105 fps 139 fps 105 fps 208 fps 70 fps
	1	320 × 480	Mono8 Mono12 Mono16	208 fps2x H-binning 208 fps2x H-binning 208 fps2x H-binning
	2	640 × 240	Mono8 Mono12 Mono16	372 fps2x V-binning 271 fps2x V-binning 208 fps2x V-binning
	3	320 × 240	Mono8 Mono12 Mono16	372 fps2x H+V binning 372 fps2x H+V binning 372 fps2x H+V binning
	4	320 × 480 320 × 480	Mono8 Mono12 Mono16 YUV411,Raw12 YUV422,Raw16 Mono8,Raw8 RGB8	208 fps2 out of 4 H-sub-sampling 208 fps2 out of 4 H-sub-sampling 208 fps2 out of 4 H-sub-sampling 208 fps2 out of 4 H-sub-sampling 208 fps2 out of 4 H-sub-sampling 208 fps2 out of 4 H-sub-sampling 139 fps2 out of 4 H-sub-sampling
	5	640 × 240 640 × 240	Mono8 Mono12 Mono16 YUV411,Raw12 YUV422,Raw16 Mono8,Raw8 RGB8	372 fps2 out of 4 V-sub-sampling 372 fps2 out of 4 V-sub-sampling 372 fps2 out of 4 V-sub-sampling 271 fps2 out of 4 V-sub-sampling 208 fps2 out of 4 V-sub-sampling 372 fps2 out of 4 V-sub-sampling 139 fps2 out of 4 V-sub-sampling
	6	320 × 240 320 × 240	Mono8 Mono12 Mono16 YUV411,Raw12 YUV422,Raw16 Mono8,Raw8 RGB8	372 fps2 out of 4 H+V sub-sampling 372 fps2 out of 4 H+V sub-sampling 372 fps2 out of 4 H+V sub-sampling 372 fps2 out of 4 H+V sub-sampling 372 fps2 out of 4 H+V sub-sampling 372 fps2 out of 4 H+V sub-sampling 271 fps2 out of 4 H+V sub-sampling

Table 85: Video Format_7 default modes Pike F-032B, Pike F-032C

Pike F-100B, F-100C

Format	Mode	Resolution	Color mode	120 fps	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444							
	1	320 × 240	YUV422	✓	✓	✓	✓	✓	✓	✓
	2	640 × 480	YUV411		✓	✔	✔	✔	✔	✓
	3	640 × 480	YUV422		✓	✔	✔	✔	✔	✓
	4	640 × 480	RGB8		✓	✔	✔	✔	✔	✓
	5	640 × 480	Mono8		✓ ✔	✓ ✔	✓ ✔	✓ ✔	✓ ✔	✓ ✔
	6	640 × 480	Mono16		✓	✓	✓	✓	✓	✓
1	0	800 × 600	YUV422		✓	✔	✔	✔	✔	
	1	800 × 600	RGB8			✔	✔	✔		
	2	800 × 600	Mono8		✓ ✔	✓ ✔	✓ ✔	✓ ✔		
	3	1024 × 768	YUV422							
	4	1024 × 768	RGB8							
	5	1024 × 768	Mono8							
	6	800 × 600	Mono16		✓	✓	✓	✓	✓	
	7	1024 × 768	Mono16							

Table 86: Video fixed formats Pike F-100B, F-100C

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	1000 × 1000 1000 × 1000	Mono8 Mono12 Mono16 YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	60 fps 43 fps 33 fps 43 fps 33 fps 60 fps 22 fps
	1	500 × 1000	Mono8 Mono12 Mono16	60 fps2x H-binning 60 fps2x H-binning 60 fps2x H-binning
	2	1000 × 500	Mono8 Mono12 Mono16	99 fps2x V-binning 86 fps2x V-binning 65 fps2x V-binning
	3	500 × 500	Mono8 Mono12 Mono16	99 fps2x H+V binning 99 fps2x H+V binning 99 fps2x H+V binning
	4	500 × 1000 500 × 1000	Mono8 Mono12 Mono16 YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	60 fps2x H-sub-sampling 60 fps2x H-sub-sampling 60 fps2x H-sub-sampling 60 fps2 out of 4 H-sub-sampling 60 fps2 out of 4 H-sub-sampling 60 fps2 out of 4 H-sub-sampling 43 fps2 out of 4 H-sub-sampling
	5	1000 × 500 1000 × 500	Mono8 Mono12 Mono16 YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	99 fps2x V-sub-sampling 86 fps2x V-sub-sampling 65 fps2x V-sub-sampling 86 fps2 out of 4 V-sub-sampling 65 fps2 out of 4 V-sub-sampling 99 fps2 out of 4 V-sub-sampling 43 fps2 out of 4 V-sub-sampling
	6	500 × 500 500 × 500	Mono8 Mono12 Mono16 YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	99 fps2x H+V-sub-sampling 99 fps2x H+V-sub-sampling 99 fps2x H+V-sub-sampling 99 fps2 out of 4 H+V-sub-sampling 99 fps2 out of 4 H+V-sub-sampling 99 fps2 out of 4 H+V-sub-sampling 86 fps2 out of 4 H+V-sub-sampling

Table 87: Video Format_7 default modes Pike F-100B, F-100C

Pike F-145B, F-145C (-15 fps**)

**Pike F-145-15fps cameras have frame rates up to 15 fps only (except color models Format_0 Mode_1: up to 30 fps).

Format	Mode	Resolution	Color mode	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444						
	1	320 × 240	YUV422	✓	✓	✓	✓	✓	✓
	2	640 × 480	YUV411		✓	✓	✓	✓	✓
	3	640 × 480	YUV422		✓	✓	✓	✓	✓
	4	640 × 480	RGB8		✓	✓	✓	✓	✓
	5	640 × 480	Mono8		✓ ✓	✓ ✓	✓ ✓	✓ ✓	✓ ✓
	6	640 × 480	Mono16		✓	✓	✓	✓	✓
1	0	800 × 600	YUV422		✓	✓	✓	✓	
	1	800 × 600	RGB8		✓	✓	✓		
	2	800 × 600	Mono8		✓ ✓	✓ ✓	✓ ✓		
	3	1024 × 768	YUV422		✓	✓	✓	✓	✓
	4	1024 × 768	RGB8			✓	✓	✓	✓
	5	1024 × 768	Mono8		✓ ✓	✓ ✓	✓ ✓	✓ ✓	✓ ✓
	6	800 × 600	Mono16		✓	✓	✓	✓	
	7	1024 × 768	Mono16		✓	✓	✓	✓	✓
2	0	1280 × 960	YUV422			✓	✓	✓	✓
	1	1280 × 960	RGB8			✓	✓	✓	✓
	2	1280 × 960	Mono 8		✓ ✓	✓ ✓	✓ ✓	✓ ✓	✓ ✓
	3	1600 × 1200	YUV422						
	4	1600 × 1200	RGB8						
	5	1600 × 1200	Mono8						
	6	1280 × 960	Mono16			✓	✓	✓	✓
	7	1600 × 1200	Mono16						

Table 88: Video fixed formats Pike F-145B, F-145C

Frame rates with shading are only achievable with IEEE1394b (S800).

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	1388 × 1038	Mono8 Mono12 Mono16	30 (16*) fps 30 (16*) fps 23 (16*) fps
		1388 × 1038	YUV411 YUV422,Raw16 Mono8,Raw8 Raw12 RGB8	30 (16*) fps 23 (16*) fps 30 (16*) fps 30 (16*) fps 15 (15*) fps
	1	692 × 1038	Mono8 Mono12 Mono16	30 (16*) fps2x H-binning 30 (16*) fps2x H-binning 30 (16*) fps2x H-binning
	2	1388 × 518	Mono8 Mono12 Mono16	51 (27*) fps2x V-binning 51 (27*) fps2x V-binning 45 (27*) fps2x V-binning
	3	692 × 518	Mono8 Mono12 Mono16	51 (27*) fps2x H+V binning 51 (27*) fps2x H+V binning 51 (27*) fps2x H+V binning
	4	692 × 1038	Mono8 Mono12 Mono16	30 (16*) fps2 out of 4 H-sub-sampling 30 (16*) fps2 out of 4 H-sub-sampling 30 (16*) fps2 out of 4 H-sub-sampling
		692 × 1038	YUV411 YUV422,Raw16 Mono8,Raw8 Raw12 RGB8	30 (16*) fps2 out of 4 H-sub-sampling 30 (16*) fps2 out of 4 H-sub-sampling 30 (16*) fps2 out of 4 H-sub-sampling 37 (16*) fps2 out of 4 H-sub-sampling 30 (16*) fps2 out of 4 H-sub-sampling
	5[#]	1388 × 518	Mono8 Mono12 Mono16	30 (16*) fps2 out of 4 V-sub-sampling 30 (16*) fps2 out of 4 V-sub-sampling 23 (16*) fps2 out of 4 V-sub-sampling
		1388 × 518	YUV411 YUV422,Raw16 Mono8,Raw8 Raw12 RGB8	30 (16*) fps2 out of 4 V-sub-sampling 23 (16*) fps2 out of 4 V-sub-sampling 30 (16*) fps2 out of 4 V-sub-sampling 37 (20*) fps2 out of 4 V-sub-sampling 15 (15*) fps2 out of 4 V-sub-sampling
	6[#]	692 × 518	Mono8 Mono12 Mono16	30 (16*) fps2 out of 4 H+V-sub-sampling 30 (16*) fps2 out of 4 V-sub-sampling 30 (16*) fps2 out of 4 H+V-sub-sampling
		692 × 518	YUV411 YUV422,Raw16 Mono8,Raw8 Raw12 RGB8	30 (16*) fps2 out of 4 H+V-sub-sampling 30 (16*) fps2 out of 4 H+V-sub-sampling 30 (16*) fps2 out of 4 H+V-sub-sampling 37 (20*) fps2 out of 4 H+V-sub-sampling 30 (16*) fps2 out of 4 H+V-sub-sampling

Table 89: Video Format_7 default modes Pike F-145B, F-145C

#:Vertical sub-sampling is done via concealing certain lines, so the frame rate is not frame rate = f (AOI height) but frame rate = f (2 × AOI height)	** applicable to 15 fps variant only

Pike F-210B

Format	Mode	Resolution	Color mode	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444					
	1	320 × 240	YUV422					
	2	640 × 480	YUV411					
	3	640 × 480	YUV422					
	4	640 × 480	RGB8					
	5	640 × 480	Mono 8	✔	✔	✔	✔	✔
	6	640 × 480	Mono 16	✔	✔	✔	✔	✔
1	0	800 × 600	YUV422					
	1	800 × 600	RGB8					
	2	800 × 600	Mono8	✔	✔	✔		
	3	1024 × 768	YUV422					
	4	1024 × 768	RGB8					
	5	1024 × 768	Mono 8	✔	✔	✔	✔	✔
	6	800 × 600	Mono16	✔	✔	✔	✔	
	7	1024 × 768	Mono16	✔ (shaded)	✔	✔	✔	✔
2	0	1280 × 960	YUV422					
	1	1280 × 960	RGB8					
	2	1280 × 960	Mono 8	✔ (shaded)	✔	✔	✔	✔
	3	1600 × 1200	YUV422					
	4	1600 × 1200	RGB8					
	5	1600 × 1200	Mono8					
	6	1280 × 960	Mono16		✔ (shaded)	✔	✔	✔
	7	1600 × 1200	Mono16					

Table 90: Video fixed formats Pike F-210B

Frame rates with shading are only achievable with IEEE1394b (S800).

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	1920 × 1080	Mono8 Mono12 Mono16	31 fps 21 fps 16 fps
	1	960 × 1080	Mono8 Mono12 Mono16	32 fps2x H-binning 32 fps2x H-binning 31 fps2x H-binning
	2	1920 × 540	Mono8 Mono12 Mono16	52 fps2x V-binning 42 fps2x V-binning 31 fps2x V-binning
	3	960 × 540	Mono8 Mono12 Mono16	52 fps2x H+V binning 52 fps2x H+V binning 52 fps2x H+V binning
	4	960 × 1080	Mono8 Mono12 Mono16	32 fps2x H-sub-sampling 32 fps2x H-sub-sampling 31 fps2x H-sub-sampling
	5#	1920 × 540	Mono8 Mono12 Mono16	31 fps2x V-sub-sampling 21 fps2x V-sub-sampling 16 fps2x V-sub-sampling
	6#	960 × 540	Mono8 Mono12 Mono16	32 fps2x H+V sub-sampling 32 fps2x H+V sub-sampling 31 fps2x H+V sub-sampling

Table 91: Video Format_7 default modes Pike F-210B

#: Vertical sub-sampling is done via concealing certain lines, so the frame rate is not

frame rate = f (AOI height)
but
frame rate = f (2 × AOI height)

Pike F-421B, F-421C

Format	Mode	Resolution	Color Mode	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444					
	1	320 × 240	YUV422	✔	✔	✔	✔	✔
	2	640 × 480	YUV411	✔	✔	✔	✔	✔
	3	640 × 480	YUV422	✔	✔	✔	✔	✔
	4	640 × 480	RGB8	✔	✔	✔	✔	✔
	5	640 × 480	Mono8	✔ ✔	✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	640 × 480	Mono16	✔	✔	✔	✔	✔
1	0	800 × 600	YUV422	✔	✔	✔	✔	
	1	800 × 600	RGB8	✔	✔	✔		
	2	800 × 600	Mono8	✔ ✔	✔ ✔	✔ ✔		
	3	1024 × 768	YUV422	✔	✔	✔	✔	✔
	4	1024 × 768	RGB8		✔	✔	✔	✔
	5	1024 × 768	Mono8	✔ ✔	✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	800 × 600	Mono16	✔	✔	✔	✔	
	7	1024 × 768	Mono16	✔	✔	✔	✔	✔
2	0	1280 × 960	YUV422		✔	✔	✔	✔
	1	1280 × 960	RGB8		✔	✔	✔	✔
	2	1280 × 960	Mono8		✔ ✔	✔ ✔	✔ ✔	✔ ✔
	3	1600 × 1200	YUV422		✔	✔	✔	✔
	4	1600 × 1200	RGB8			✔	✔	✔
	5	1600 × 1200	Mono8		✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	1280 × 960	Mono16		✔	✔	✔	✔
	7	1600 × 1200	Mono16		✔	✔	✔	✔

Table 92: Video fixed formats Pike F-421B, F-421C

Frame rates with shading are only achievable with IEEE1394b (S800).

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color Mode	Maximum S800 frame rates for Format_7 modes
7	0	2048 × 2048	Mono8 Mono12 Mono16	16 fps 10 fps 8 fps
		2048 × 2048	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	10 fps 8 fps 16 fps 5 fps
	1	1024 × 2048	Mono8 Mono12 Mono16	16 fps2x H-binning 16 fps2x H-binning 16 fps2x H-binning
	2	2048 × 1024	Mono8 Mono12 Mono16	29 fps2x V-binning 21 fps2x V-binning 16 fps2x V-binning
	3	1024 × 1024	Mono8 Mono12 Mono16	29 fps2x H+V binning 29 fps2x H+V binning 29 fps2x H+V binning
	4	1024 × 2048	Mono8 Mono12 Mono16	16 fps2x H-sub-sampling 16 fps2x H-sub-sampling 16 fps2x H-sub-sampling
		1024 × 2048	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	16 fps2 out of 4 H-sub-sampling 16 fps2 out of 4 H-sub-sampling 16 fps2 out of 4 H-sub-sampling 10 fps2 out of 4 H-sub-sampling
	5	2048 × 1024	Mono8 Mono12 Mono16	29 fps2 out of 4 V-sub-sampling 21 fps2 out of 4 V-sub-sampling 16 fps2 out of 4 V-sub-sampling
		2048 × 1024	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	29 fps2 out of 4 V-sub-sampling 21 fps2 out of 4 V-sub-sampling 29 fps2 out of 4 V-sub-sampling 10 fps2 out of 4 V-sub-sampling
	6	1024 × 1024	Mono8 Mono12 Mono16	29 fps2 out of 4 H+V-sub-sampling 29 fps2 out of 4 H+V-sub-sampling 29 fps2 out of 4 H+V-sub-sampling
		1024 × 1024	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8	29 fps2 out of 4 H+V-sub-sampling 29 fps2 out of 4 H+V-sub-sampling 29 fps2 out of 4 H+V-sub-sampling 21 fps2 out of 4 H+V-sub-sampling

Table 93: Video Format_7 default modes Pike F-421B, F-421C

Pike F-505B, F-505C

Format	Mode	Resolution	Color mode	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444					
	1	320 × 240	YUV422	✔	✔	✔	✔	✔
	2	640 × 480	YUV411	✔	✔	✔	✔	✔
	3	640 × 480	YUV422	✔	✔	✔	✔	✔
	4	640 × 480	RGB8	✔	✔	✔	✔	✔
	5	640 × 480	Mono8	✔ ✔	✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	640 × 480	Mono16	✔	✔	✔	✔	✔
1	0	800 × 600	YUV422		✔	✔	✔	
	1	800 × 600	RGB8		✔	✔		
	2	800 × 600	Mono8		✔ ✔	✔ ✔		
	3	1024 × 768	YUV422		✔	✔	✔	✔
	4	1024 × 768	RGB8		✔	✔	✔	✔
	5	1024 × 768	Mono8		✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	800 × 600	Mono16		✔	✔	✔	
	7	1024 × 768	Mono16		✔	✔	✔	✔
2	0	1280 × 960	YUV422		✔	✔	✔	✔
	1	1280 × 960	RGB8		✔	✔	✔	✔
	2	1280 × 960	Mono 8		✔ ✔	✔ ✔	✔ ✔	✔ ✔
	3	1600 × 1200	YUV422		✔	✔	✔	✔
	4	1600 × 1200	RGB8			✔	✔	✔
	5	1600 × 1200	Mono8		✔ ✔	✔ ✔	✔ ✔	✔ ✔
	6	1280 × 960	Mono16		✔	✔	✔	✔
	7	1600 × 1200	Mono16		✔	✔	✔	✔

Table 94: Video fixed formats Pike F-505B, F-505C

Frame rates with shading are only achievable with IEEE1394b (S800).

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	2452 × 2054	Mono8 Mono12 Mono16	13 fps 09 fps 07 fps
		2452 × 2054	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	09 fps 07 fps 13 fps 04 fps 09 fps
	1	1224 × 2054	Mono8 Mono12 Mono16	15 fps2x H-binning 15 fps2x H-binning 13 fps2x H-binning
	2	2452 × 1026	Mono8 Mono12 Mono16	22 fps2x V-binning 17 fps2x V-binning 13 fps2x V-binning
	3	1224 × 1026	Mono8 Mono12 Mono16	22 fps2x H+V binning 22 fps2x H+V binning 22 fps2x H+V binning
	4	1224 × 2054	Mono8 Mono12 Mono16	15 fps2 out of 4 H-sub-sampling 15 fps2 out of 4 H-sub-sampling 13 fps2 out of 4 H-sub-sampling
		1224 × 2054	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	15 fps2 out of 4 H-sub-sampling 13 fps2 out of 4 H-sub-sampling 15 fps2 out of 4 H-sub-sampling 09 fps2 out of 4 H-sub-sampling 15 fps2 out of 4 H-sub-sampling
	5	2452 × 1026	Mono8 Mono12 Mono16	22 fps2 out of 4 V-sub-sampling 17 fps2 out of 4 V-sub-sampling 13 fps2 out of 4 V-sub-sampling
		2452 × 1026	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	17 fps2 out of 4 V-sub-sampling 13 fps2 out of 4 V-sub-sampling 22 fps2 out of 4 V-sub-sampling 09 fps2 out of 4 V-sub-sampling 17 fps2 out of 4 V-sub-sampling
	6	1224 × 1026	Mono8 Mono12 Mono16	22 fps2 out of 4 H+V-sub-sampling 22 fps2 out of 4 H+V-sub-sampling 22 fps2 out of 4 H+V-sub-sampling
		1224 × 1026	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	22 fps2 out of 4 H+V-sub-sampling 22 fps2 out of 4 H+V-sub-sampling 22 fps2 out of 4 H+V-sub-sampling 17 fps2 out of 4 H+V-sub-sampling 22 fps2 out of 4 H+V-sub-sampling

Table 95: Video Format_7 default modes Pike F-505B, F-505C

Pike F-1100B, F-1100C

Format	Mode	Resolution	Color mode	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444				
	1	320 × 240	YUV422	✓ *	✓	✓	✓
	2	640 × 480	YUV411	✓ *	✓	✓	✓
	3	640 × 480	YUV422	✓ *	✓	✓	✓
	4	640 × 480	RGB8	✓ *	✓	✓	✓
	5	640 × 480	Mono8	✔ * ✓ *	✔ ✓	✔ ✓	✔ ✓
	6	640 × 480	Mono16	✔ *	✔	✔	
1	0	800 × 600	YUV422		✓	✓	
	1	800 × 600	RGB8		✓		
	2	800 × 600	Mono8		✔ ✓		
	3	1024 × 768	YUV422		✓ *	✓	✓
	4	1024 × 768	RGB8		✓ *	✓	✓
	5	1024 × 768	Mono8		✔ * ✓ *	✔ ✓	✔ ✓
	6	800 × 600	Mono16		✔	✔	
	7	1024 × 768	Mono16		✔ *	✔	✔
2	0	1280 × 960	YUV422		✓ *	✓	✓
	1	1280 × 960	RGB8		✓ *	✓	✓
	2	1280 × 960	Mono 8		✔ * ✓ *	✔ ✓	✔ ✓
	3	1600 × 1200	YUV422		✓ *	✓	✓
	4	1600 × 1200	RGB8		✓ *	✓	✓
	5	1600 × 1200	Mono8		✔ * ✓ *	✔ ✓	✔ ✓
	6	1280 × 960	Mono16		✔ *	✔	✔
	7	1600 × 1200	Mono16		✔ *	✔	✔

Table 96: Video fixed formats Pike F-1100B, F-1100C

✔ * ✓ * Frame rates with asterisk * are only achievable in dual-tap mode.

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	4008 × 2672	Mono8 Mono12 Mono16	4.9 fps 4.9 fps 4.1 fps
		4008 × 2672	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	4.9 fps 4.1 fps 4.9 fps 2.7 fps 4.9 fps
	1	2004 × 2672	Mono8 Mono12 Mono16	4.9 fps2x H-binning 4.9 fps2x H-binning 4.9 fps2x H-binning
	2	4008 × 1336	Mono8 Mono12 Mono16	8.5 fps2x V-binning 8.5 fps2x V-binning 8.2 fps2x V-binning
	3	2004 × 1336	Mono8 Mono12 Mono16	8.5 fps2x H+V binning 8.5 fps2x H+V binning 8.5 fps2x H+V binning
	4	2004 × 2672	Mono8 Mono12 Mono16	3.5 fps2 out of 4 H-sub-sampling 3.5 fps2 out of 4 H-sub-sampling 3.5 fps2 out of 4 H-sub-sampling
		2004 × 2672	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	3.5 fps2 out of 4 H-sub-sampling 3.5 fps2 out of 4 H-sub-sampling 3.5 fps2 out of 4 H-sub-sampling 3.5 fps2 out of 4 H-sub-sampling 3.5 fps2 out of 4 H-sub-sampling
	5	4008 × 1336	Mono8 Mono12 Mono16	3.5 fps2 out of 4 V-sub-sampling 3.5 fps2 out of 4 V-sub-sampling 3.5 fps2 out of 4 V-sub-sampling
		4008 × 1336	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	3.5 fps2 out of 4 V-sub-sampling 3.5 fps2 out of 4 V-sub-sampling 3.5 fps2 out of 4 V-sub-sampling 2.7 fps2 out of 4 V-sub-sampling 3.5 fps2 out of 4 V-sub-sampling
	6	2004 × 1336	Mono8 Mono12 Mono16	6.3 fps2 out of 4 H+V-sub-sampling 6.3 fps2 out of 4 H+V-sub-sampling 6.3 fps2 out of 4 H+V-sub-sampling
		2004 × 1336	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	6.3 fps2 out of 4 H+V-sub-sampling 6.3 fps2 out of 4 H+V-sub-sampling 6.3 fps2 out of 4 H+V-sub-sampling 6.3 fps2 out of 4 H+V-sub-sampling 6.3 fps2 out of 4 H+V-sub-sampling

Table 97: Video Format_7 default modes Pike F-1100B, F-1100C [dual-tap, maxBPP=11000]

Pike F-1600B, F-1600C

Format	Mode	Resolution	Color mode	7.5 fps	3.75 fps	1.875 fps
0	0	160 × 120	YUV444			
	1	320 × 240	YUV422			
	2	640 × 480	YUV411	✓	✓	✓
	3	640 × 480	YUV422	✓	✓	✓
	4	640 × 480	RGB8	✓	✓	✓
	5	640 × 480	Mono8	✓ ✓	✓ ✓	✓ ✓
	6	640 × 480	Mono16	✓	✓	✓
1	0	800 × 600	YUV422	✓ *	✓	
	1	800 × 600	RGB8	✓ *		
	2	800 × 600	Mono8	✓ * ✓ *		
	3	1024 × 768	YUV422	✓ *	✓	✓
	4	1024 × 768	RGB8	✓ *	✓	✓
	5	1024 × 768	Mono8	✓ * ✓ *	✓ ✓	✓ ✓
	6	800 × 600	Mono16	✓ *	✓	
	7	1024 × 768	Mono16	✓ *	✓	✓
2	0	1280 × 960	YUV422	✓ *	✓	✓
	1	1280 × 960	RGB8	✓ *	✓	✓
	2	1280 × 960	Mono 8	✓ * ✓ *	✓ ✓	✓ ✓
	3	1600 × 1200	YUV422		✓	✓
	4	1600 × 1200	RGB8		✓	✓
	5	1600 × 1200	Mono8		✓ ✓	✓ ✓
	6	1280 × 960	Mono16	✓ *	✓	✓
	7	1600 × 1200	Mono16		✓	✓

Table 98: Video fixed formats Pike F-1600B, F-1600C

✓ * ✓ * Frame rates with asterisk * are only achievable in dual-tap mode.

Note

The following Format_7 tables show default Format_7 modes without Format_7 mode mapping.

- see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152
- see Format_7 mode mapping on page 322

Format	Mode	Resolution	Color mode	Maximum S800 frame rates for Format_7 modes
7	0	4872 × 3248	Mono8 Mono12 Mono16	3.1 fps 3.1 fps 2.7 fps
		4872 × 3248	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	3.1 fps 2.7 fps 3.1 fps 1.8 fps 3.1 fps
	1	2436 × 3248	Mono8 Mono12 Mono16	3.1 fps2x H-binning 3.1 fps2x H-binning 3.1 fps2x H-binning
	2	4872 × 1624	Mono8 Mono12 Mono16	5.5 fps2x V-binning 5.5 fps2x V-binning 5.5 fps2x V-binning
	3	2436 × 1624	Mono8 Mono12 Mono16	5.3 fps2x H+V binning 5.3 fps2x H+V binning 5.3 fps2x H+V binning
	4	2436 × 3248	Mono8 Mono12 Mono16	2.2 fps2 out of 4 H-sub-sampling 2.2 fps2 out of 4 H-sub-sampling 2.2 fps2 out of 4 H-sub-sampling
		2436 × 3248	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	2.2 fps2 out of 4 H-sub-sampling 2.2 fps2 out of 4 H-sub-sampling 2.2 fps2 out of 4 H-sub-sampling 2.2 fps2 out of 4 H-sub-sampling 2.2 fps2 out of 4 H-sub-sampling
	5	4872 × 1624	Mono8 Mono12 Mono16	4.0 fps2 out of 4 V-sub-sampling 4.0 fps2 out of 4 V-sub-sampling 4.0 fps2 out of 4 V-sub-sampling
		4872 × 1624	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	4.0 fps2 out of 4 V-sub-sampling 4.0 fps2 out of 4 V-sub-sampling 4.0 fps2 out of 4 V-sub-sampling 3.7 fps2 out of 4 V-sub-sampling 4.0 fps2 out of 4 V-sub-sampling
	6	2436 × 1624	Mono8 Mono12 Mono16	4.0 fps2 out of 4 H+V-sub-sampling 4.0 fps2 out of 4 H+V-sub-sampling 4.0 fps2 out of 4 H+V-sub-sampling
		2436 × 1624	YUV411 YUV422,Raw16 Mono8,Raw8 RGB8 Raw12	4.0 fps2 out of 4 H+V-sub-sampling 4.0 fps2 out of 4 H+V-sub-sampling 4.0 fps2 out of 4 H+V-sub-sampling 4.0 fps2 out of 4 H+V-sub-sampling 4.0 fps2 out of 4 H+V-sub-sampling

Table 99: Video Format_7 default modes Pike F-1600B, F-1600C [dual-tap, maxBPP=11000]

Area of interest (AOI)

The camera's image sensor has a defined resolution. This indicates the maximum number of lines and pixels per line that the recorded image may have.

However, often only a certain section of the entire image is of interest. The amount of data to be transferred can be decreased by limiting the image to a section when reading it out from the camera. At a lower vertical resolution the sensor can be read out faster and thus the frame rate is increased.

Note

The setting of AOIs is supported only in video Format_7.

While the size of the image read out for most other video formats and modes is fixed by the IIDC specification, thereby determining the highest possible frame rate, in Format_7 mode the user can set the upper left corner and width and height of the section (area of interest = AOI) he is interested in to determine the size and thus the highest possible frame rate.

Setting the AOI is done in the IMAGE_POSITION and IMAGE_SIZE registers.

Note

Pay attention to the increments entered in the UNIT_SIZE_INQ and UNIT_POSITION_INQ registers when configuring IMAGE_POSITION and IMAGE_SIZE.

AF_AREA_POSITION and AF_AREA_SIZE contain in the respective bits values for the column and line of the upper left corner and values for the width and height.

Note

For more information see Table 152: Format_7 control and status register on page 285.

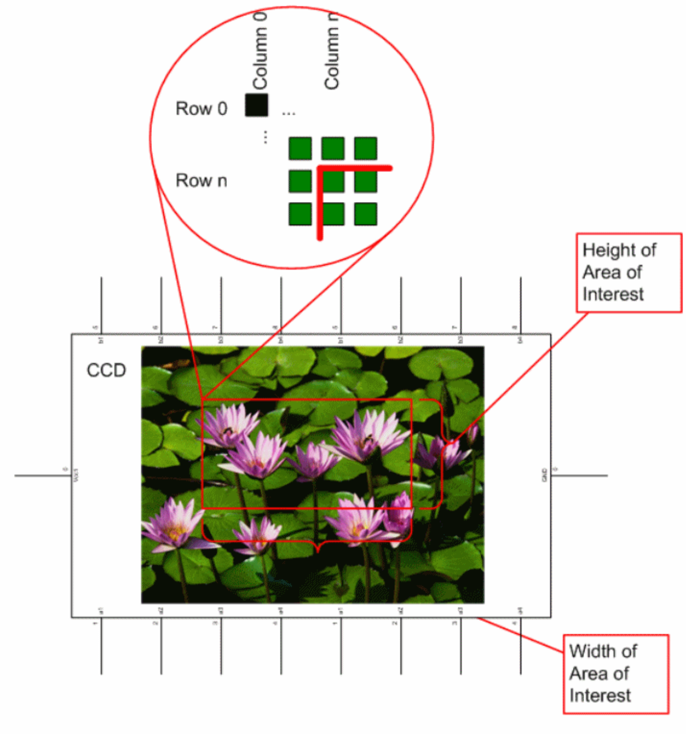


Figure 86: Area of interest (AOI)

Note

- The left position + width and the upper position + height may not exceed the maximum resolution of the sensor.
- The coordinates for width and height must be divisible by 4.

In addition to the AOI, some other parameters have an effect on the maximum frame rate:

- the time for reading the image from the sensor and transporting it into the FRAME_BUFFER
- the time for transferring the image over the FireWire™ bus
- the length of the exposure time.

Autofunction AOI

Use this feature to select the image area (work area) on which the following autofunctions work:

- Auto shutter
- Auto gain
- Auto white balance

In the following screenshot you can see an example of the autofunction AOI:

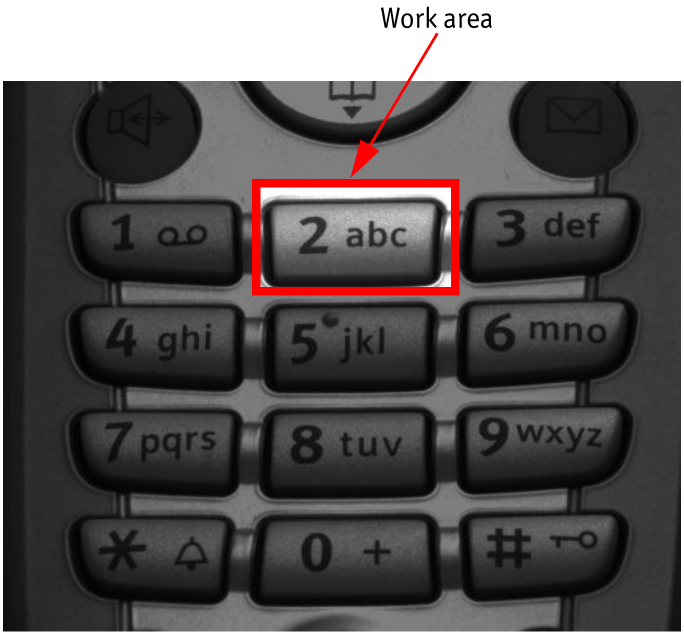


Figure 87: Example of autofunction AOI (Show work area is on)

Note

Autofunction AOI is independent from Format_7 AOI settings.

If you switch off autofunction AOI, work area position and work area size follow the current active image size.

To switch off autofunctions, carry out following actions in the order shown:

1. Uncheck Show AOI check box (SmartView Ctrl2 tab).
2. Uncheck Enable check box (SmartView Ctrl2 tab).
Switch off Auto modi (e.g. Shutter and/or Gain) (SmartView Ctrl2 tab).

As a reference it uses a grid of up to 65534 sample points equally spread over the AOI.

Note

Configuration

To configure this feature in an advanced register see Autofunction AOI on page 310.

Frame rates

An IEEE1394 camera requires bandwidth to transport images.

The IEEE1394b bus has very large bandwidth of at least 62.5 MByte/s for transferring (isochronously) image data. Per cycle up to 8192 bytes (or around 2000 quadlets = 4 bytes@ 800 Mbit/s) can thus be transmitted.

Note

All bandwidth data is calculated with:

1 MByte = 1024 KB

Depending on the video format settings and the configured frame rate, the camera requires a certain percentage of maximum available bandwidth. Clearly the bigger the image and the higher the frame rate, the more data is to be transmitted.

The following tables indicate the volume of data in various formats and modes to be sent within one cycle (125 µs) at 800 Mbit/s of bandwidth.

The tables are divided into three formats:

Format	Resolution	Max. Video Format
Format_0	up to VGA	640 × 480
Format_1	up to XGA	1024 × 768
Format_2	up to UXGA	1600 × 1200

Table 100: Overview fixed formats

They enable you to calculate the required bandwidth and to ascertain the number of cameras that can be operated independently on a bus and in which mode.

Format	Mode	Resolution	240 fps	120 fps	60 fps	30 fps	15 fps	7.5 fps	3.75 fps
0	0	160 × 120 YUV (4:4:4) 24 bit/pixel	4H 640p 480q	2H 320p 240q	1H 160p 120q	1/2H 80p 60q	1/4H 40p 30q	1/8H 20p 15q	
	1	320 × 240 YUV (4:2:2) 16 bit/pixel	8H 2560p 1280q	4H 1280p 640q	2H 640p 320q	1H 320p 160q	1/2H 160p 80q	1/4H 80p 40q	1/8H 40p 20q
	2	640 × 480 YUV (4:1:1) 12 bit/pixel		8H 5120p 1920q	4H 2560p 960q	2H 1280p 480q	1H 640p 240q	1/2H 320p 120q	1/4H 160p 60q
	3	640 × 480 YUV (4:2:2) 16 bit/pixel			4H 2560p 1280q	2H 1280p 640q	1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q
	4	640 × 480 RGB 24 bit/pixel			4H 2560p 1280q	2H 1280p 960q	1H 640p 480q	1/2H 320p 240q	1/4H 160p 120q
	5	640 × 480 (Mono8) 8 bit/pixel		8H 5120p 1280q	4H 2560p 640q	2H 1280p 320q	1H 640p 160q	1/2H 320p 80q	1/4H 160 p40q
	6	640 × 480 Y (Mono16) 16 Bit/pixel			4H 2560p 1280q	2H 1280p 640q	1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q
	7	Reserved							

Table 101: Format_0

As an example, VGA Mono8 @ 60 fps requires four lines (640 × 4 = 2560 pixels/byte) to transmit every 125 µs: this is a consequence of the sensor's line time of about 30 µs, so that no data needs to be stored temporarily.

It takes 120 cycles (120 × 125 µs = 15 ms) to transmit one frame, which arrives every 16.6 ms from the camera. Again no data need to be stored temporarily.

Thus around 64% of the available bandwidth (at S400) is used. Thus one camera can be connected to the bus at S400.

The same camera, run at S800 would require only 32% of the available bandwidth, due to the doubled speed. Thus up to three cameras can be connected to the bus at S800.

Format	Mode	Resolution	240 fps	120 fps	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
1	0	800 × 600 YUV (4:2:2) 16 bit/pixel			5H 4000p 2000q	5/2H 2000p 1000q	5/4H 1000p 500q	5/8H 500p 250q	6/16H 250p 125q	
	1	800 × 600 RGB 24 bit/pixel				5/2H 2000p 1500q	5/4H 1000p 750q	5/8H 500p 375q		
	2	800 × 600 Y (Mono8) 8 bit/pixel		10H 8000p 2000q	5H 4000p 1000q	5/2H 2000p 500q	5/4H 1000p 250q	5/8H 500p 125q		
	3	1024 × 768 YUV (4:2:2) 16 bit/pixel				3H 3072p 1536q	3/2H 1536p 768q	3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q
	4	1024 × 768 RGB 24 bit/pixel					3/2H 1536p 384q	3/4H 768p 576q	3/8H 384p 288q	3/16H 192p 144q
	5	1024 × 768 Y (Mono) 8 bit/pixel			6H 6144p 1536q	3H 3072p 768q	3/2H 1536p 384q	3/4H 768p 192q	3/8H 384p 96q	3/16H 192p 48q
	6	800 × 600 (Mono16) 16 bit/pixel			5H 4000p 2000q	5/2H 2000p 1000q	5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
	7	1024 × 768 Y (Mono16) 16 bit/pixel				3H 3072p 1536q	3/2H 1536p 768q	3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q

Table 102: Format_1

Format	Mode	Resolution	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
2	0	1280 × 960 YUV (4:2:2) 16 bit/pixel			2H 2560p 1280q	1H 1280p 640q	1/2H 640p 320q	1/4H 320p 160q
	1	1280 × 960 RGB 24 bit/pixel			2H 2560p 1920q	1H 1280p 960q	1/2H 640p 480q	1/4H 320p 240q
	2	1280 × 960 Y (Mono8) 8 bit/pixel		4H 5120p 1280q	2H 2560p 640q	1H 1280p 320q	1/2H 640p 160q	1/4H 320p 80q
	3	1600 × 1200 YUV(4:2:2) 16 bit/pixel			5/2H 4000p 2000q	5/4H 2000p 1000q	5/8H 1000p 500q	5/16H 500p 250q
	4	1600 × 1200 RGB 24 bit/pixel				5/4H 2000p 1500q	5/8H 1000p 750q	5/16 500p 375q
	5	1600 × 1200 Y (Mono) 8 bit/pixel		5H 8000p 2000q	5/2H 4000p 1000q	5/4H 2000p 500q	5/8H 1000p 250q	5/16H 500p 125q
	6	1280 × 960 Y (Mono16) 16 bit/pixel			2H 2560p 1280q	1H 1280p 640q	1/2H 640p 320q	1/4H 320p 160q
	7	1600 × 1200Y(Mono16) 16 bit/pixel			5/2H 4000p 2000q	5/4H 2000p 1000q	5/8H 1000p 500q	5/16H 500p 250q

Table 103: Format_2

As already mentioned, the recommended limit for transferring isochronous image data is 2000q (quadlets) per cycle or 8192 bytes (with 800 Mbit/s of bandwidth).

Note

- If the cameras are operated with an external trigger the maximum trigger frequency may not exceed the highest continuous frame rate, so preventing frames from being dropped or corrupted.
- IEEE1394 adapter cards with PCILynx™ chipsets (predecessor of OHCI) have a limit of 4000 bytes per cycle.

The frame rates in video modes 0 to 2 are specified and set fixed by IIDC V1.31.

Frame rates Format_7

In video Format_7 frame rates are no longer fixed.

Note

- Different values apply for the different sensors.
- Frame rates may be further limited by longer shutter times and/or bandwidth limitation from the IEEE1394 bus.

Details are described in the next chapters:

- Maximum frame rate of CCD (theoretical formula)
- Diagram of frame rates as function of AOI by constant width: the curves describe RAW8, RAW12/YUV411, RAW16/YUV422, RGB8 and maximum frame rate of CCD
- Table with maximum frame rates as function of AOI by constant width

Note

CCD =theoretical maximum frame rate (in fps) of CCD according to given formula

maxBPP=8192 according to IIDC V1.31

maxBPP:for explanation and configuration see Maximum ISO packet size on page 315

Pike F-032: AOI frame rates

$$\text{Max. frame rate of CCD} = \frac{1}{69.3\mu s + \text{AOI height} \times 9.81\mu s + (490 - \text{AOI height}) \times 0.81\mu s}$$

Formula 6: Theoretical max. frame rate of CCD

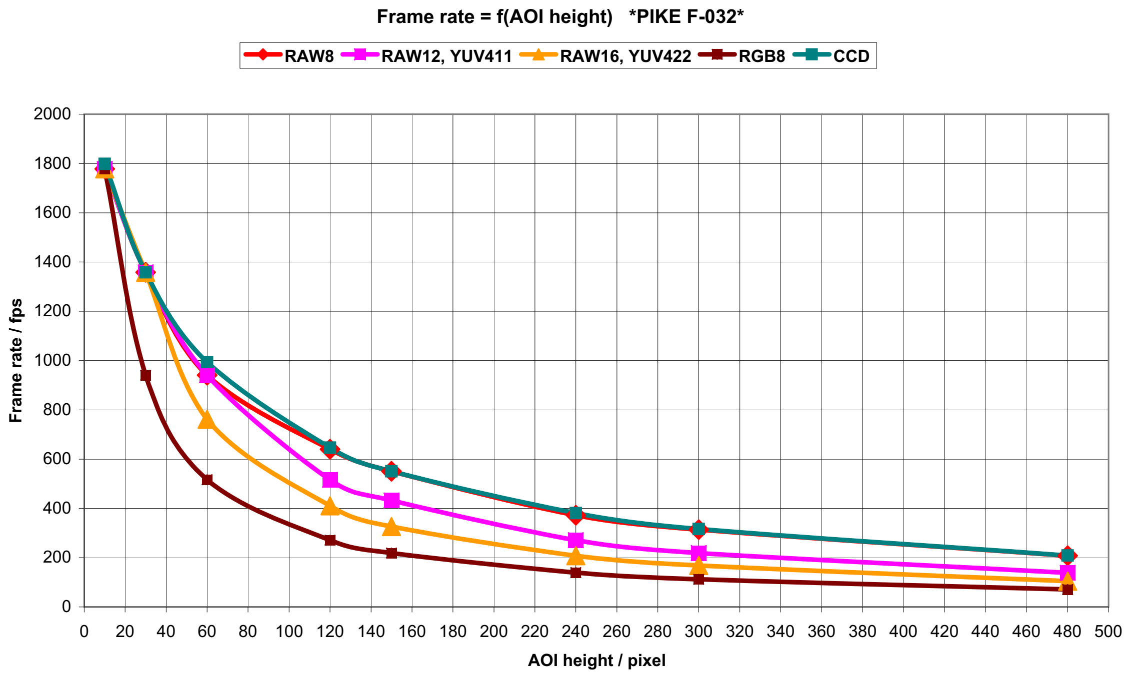


Figure 88: Frame rates as function of AOI height [width=640]

AOI height	CCD	Raw8	Raw12	Raw16	YUV411	YUV422	RGB8
480	208.93	208	139	105	139	105	70
300	315.84	314	219	168	219	168	112
240	380.78	372	271	208	271	208	139
150	550.60	550	432	327	432	327	219
120	646.75	640	516	410	516	410	271
60	993.84	941	941	762	941	762	516
30	1358.33	1358	1358	1358	1358	1358	941
10	1797.91	1778	1778	1778	1778	1778	1778

Table 104: Frame rates as function of AOI height [width=640]

Pike F-100: AOI frame rates

$$\text{Max. frame rate of CCD} = \frac{1}{174\mu s + \text{AOI height} \times 16.40\mu s + (1008 - \text{AOI height}) \times 3.4\mu s}$$

Formula 7: Theoretical max. frame rate of CCD

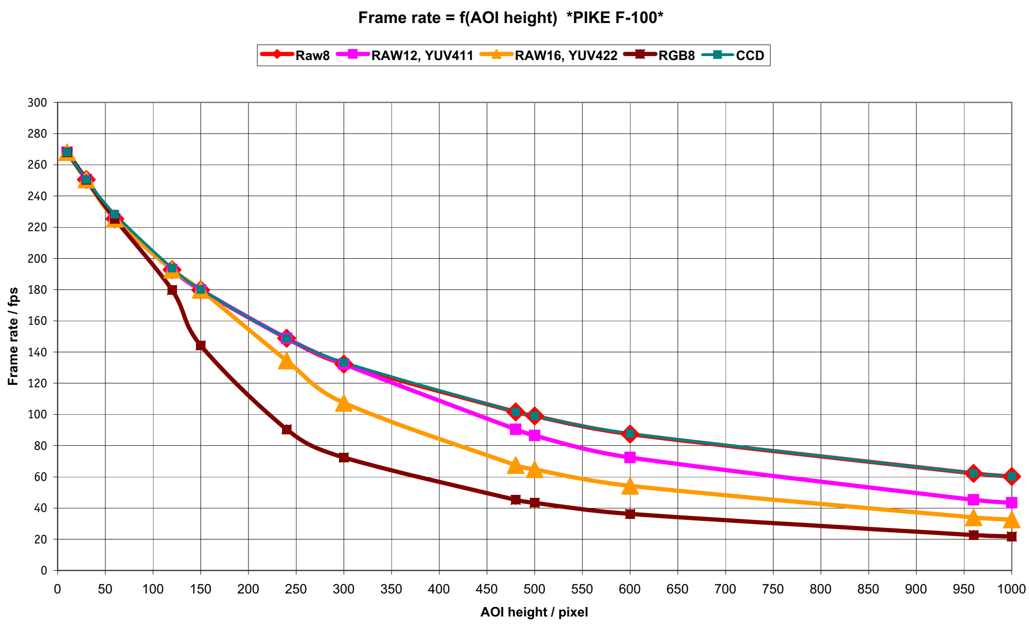


Figure 89: Frame rates as function of AOI height [width=1000]

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
1000	60.24	60	43	33	43	33	22
960	62.18	62	45	34	45	34	23
600	87.71	87	72	54	72	54	36
500	99.00	99	86	65	86	65	43
480	101.61	101	90	68	90	68	45
300	133.31	132	132	107	132	107	72
240	148.78	148	148	134	148	134	90
150	180.14	180	180	180	180	180	144
120	193.75	193	193	193	193	193	180
60	228.25	225	225	225	225	225	225
30	250.55	250	250	250	250	250	250
10	268.01	268	268	268	268	268	268

Table 105: Frame rates as function of AOI height [width=1000]

Pike F-145: AOI frame rates (no sub-sampling)

$$\text{max. frame rate of CCD} = \frac{1}{242\mu s + \text{AOI height} \times 31.80\mu s + (1051 - \text{AOI height}) \times 5.85\mu s}$$

Formula 8: Theoretical max. frame rate of CCD (no sub-sampling)

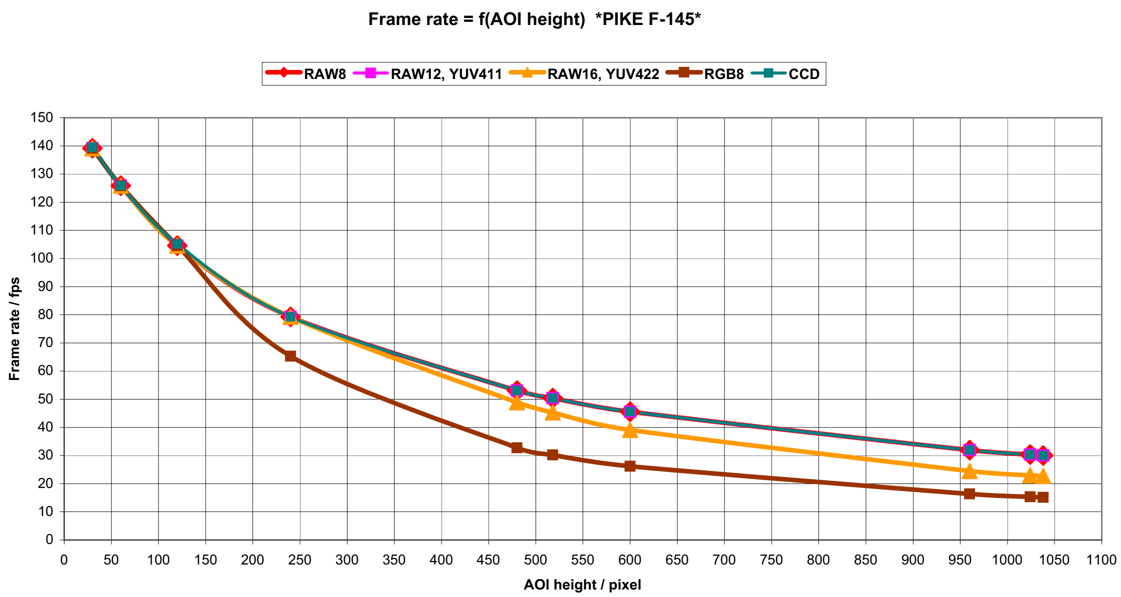


Figure 90: Frame rates as function of AOI height [width=1388]

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
1038	30.01	30	30	23	30	23	15
1024	30.34	30	30	23	30	23	15
960	31.95	31	31	25	31	25	16
600	45.54	45	45	39	45	39	26
518	50.42	50	50	45	50	45	30
480	53.06	53	53	49	53	49	33
240	79.25	79	79	79	79	79	65
120	105.21	105	105	105	105	105	105
60	125.83	125	125	125	125	125	125
30	139.49	139	139	139	139	139	139

Table 106: Frame rates as function of AOI height) [width=1388]

Pike F-145: AOI frame rates (sub-sampling)

$$\text{Max. frame rate of CCD} = \frac{1}{242\mu s + \text{AOI height} \times 1.5 \times 31.80\mu s + (1051 - \text{AOI height} \times 1.5) \times 5.85\mu s}$$

Formula 9: Theoretical max. frame rate of CCD (sub-sampling)

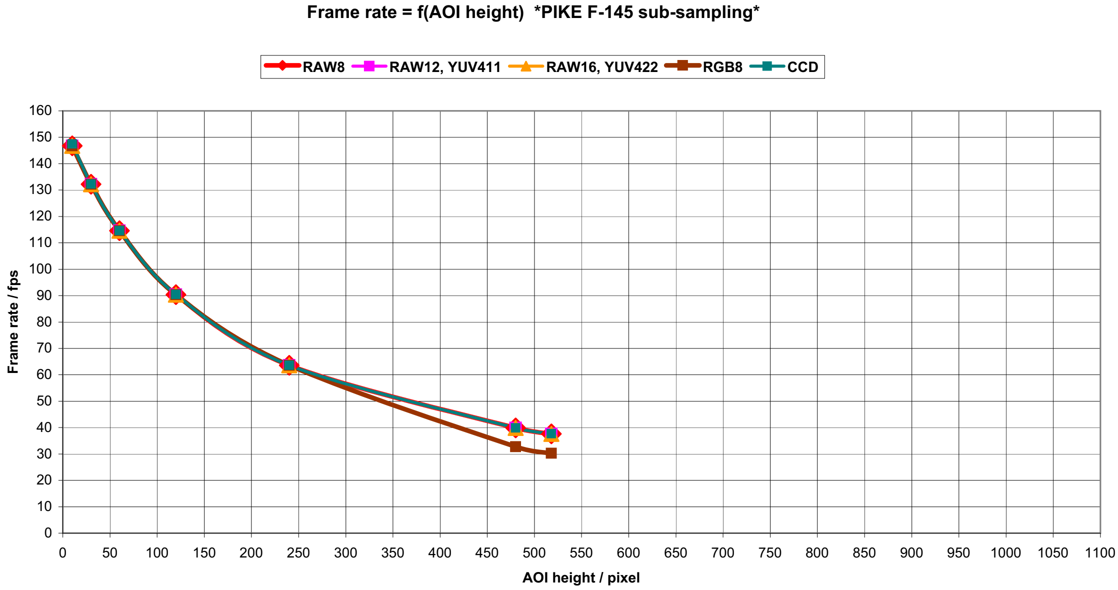


Figure 91: Frame rates as function of AOI height [width=1388] (sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
518	37.66	37	37	37	37	37	30
480	39.88	39	39	39	39	39	33
240	63.56	63	63	63	63	63	63
120	90.40	90	90	90	90	90	90
60	114.60	114	114	114	114	114	114
30	132.31	132	132	132	132	132	132
10	147.50	147	147	147	147	147	147

Table 107: Frame rates as function of AOI height [width=1388] (sub-sampling)

Pike F-145-15fps: AOI frame rates (no sub-sampling)

$$\text{Max. frame rate of CCD} = \frac{1}{450\mu s + \text{AOI height} \times 59.36\mu s + (1051 - \text{AOI height}) \times 10.92\mu s}$$

Formula 10: Theoretical max. frame rate of CCD (no sub-sampling)

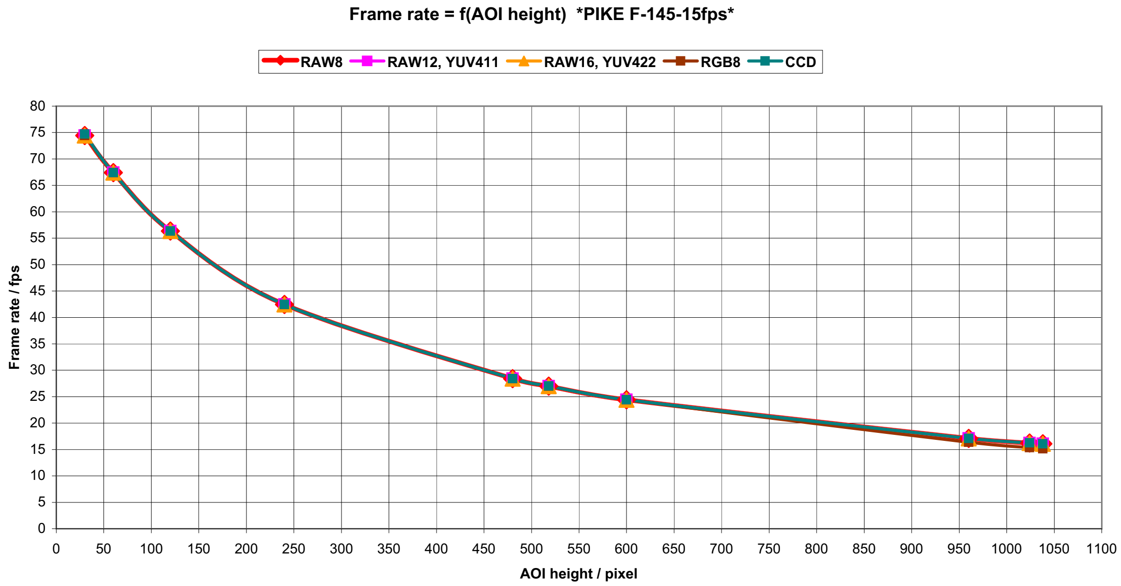


Figure 92: Frame rates as function of AOI height [width=1388]

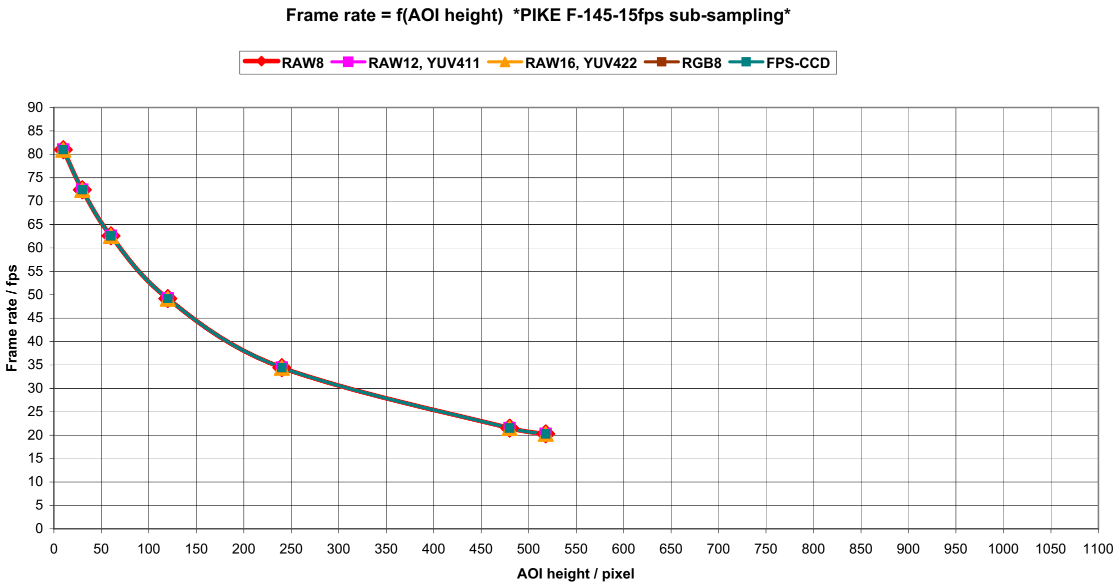
AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
1038	16.08	16	16	16	16	16	15
1024	16.25	16	16	16	16	16	15
960	17.11	17	17	17	17	17	16
600	24.40	24	24	24	24	24	24
518	27.01	27	27	27	27	27	27
480	28.43	28	28	28	28	28	28
240	42.46	42	42	42	42	42	42
120	56.37	56	56	56	56	56	56
60	67.42	67	67	67	67	67	67
30	74.74	74	74	74	74	74	74

Table 108: Frame rates as function of AOI height [width=1388]

Pike F-145-15fps: AOI frame rates (sub-sampling)

$$\text{Max. frame rate of CCD} = \frac{1}{450\mu s + \text{AOI height} \times 1.5 \times 59.36\mu s + (1051 - \text{AOI height} \times 1.5) \times 10.92\mu s}$$

Formula 11: Theoretical max. frame rate of CCD (sub-sampling)



Formula 12: Frame rates as function of AOI height [width=1388] (sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
518	20.18	20	20	20	20	20	20
480	21.37	21	21	21	21	21	21
240	34.05	34	34	34	34	34	34
120	48.44	48	48	48	48	48	48
60	61.40	61	61	61	61	61	61
30	70.89	70	70	70	70	70	70
10	79.03	79	79	79	79	79	79

Table 109: Frame rates as function of AOI height [width=1388] (sub-sampling)

Pike F-210: AOI frame rates (no sub-sampling)

$$\text{Max. frame rate of CCD} = \frac{1}{107\mu s + \text{AOI height} \times 28.6\mu s + (1092 - \text{AOI height}) \times 6.75\mu s}$$

Formula 13: Theoretical max. frame rate of CCD (no sub-sampling)

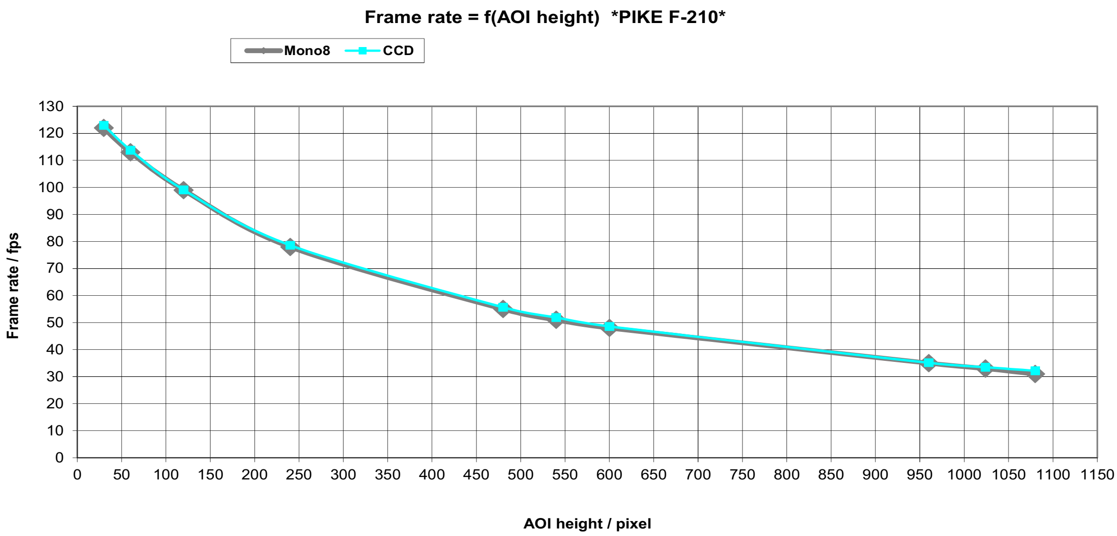


Table 110: Frame rates as function of AOI height [width=1000] (no sub-sampling)

AOI height	CCD	Mono8
1080	32.18	31
1024	33.50	33
960	35.14	35
600	48.57	48
540	51.88	51
480	56.66	55
240	78.60	78
120	99.01	99
60	113.78	113
30	122.95	122

Table 111: Frame rates as function of AOI height [width=1000] (no sub-sampling)

Pike F-210: AOI frame rates (sub-sampling)

This camera does not support a speed increase with sub-sampling.

To calculate the achievable frame rates:

Multiply the current image height by the sub-sampling factor, e.g.

- × 2 for 2 out of 4
- × 4 for 2 out of 8
- × 8 for 2 out of 16

No	Sub-sampling		
sub-sampling	2 out of 4	2 out of 8	2 out of 16
AOI height × 1	AOI height × 2	AOI height × 4	AOI height × 8
	At this mode, the camera is as fast as the camera with no sub-sampling and 2 × AOI height.	At this mode, the camera is as fast as the camera with no sub-sampling and 4 × AOI height.	At this mode, the camera is as fast as the camera with no sub-sampling and 8 × AOI height

Table 112: Frame rates for sub-sampling

Pike F-421: AOI frame rates

$$\text{Max. frame rate of CCD} = \frac{1}{125.2\mu s + \text{AOI height} \times 30.10\mu s + (2072 - \text{AOI height}) \times 3.37\mu s}$$

Formula 14: Theoretical max. frame rate of CCD

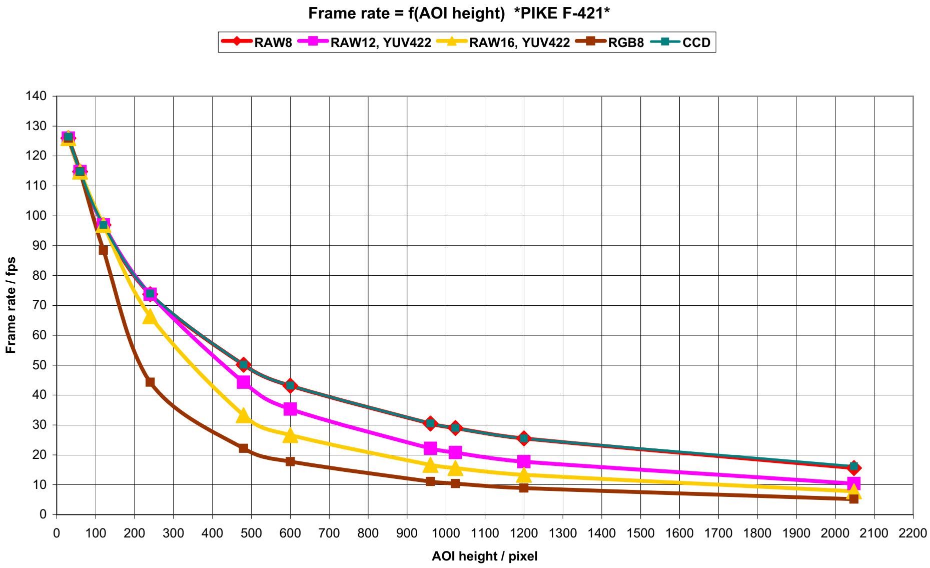


Table 113: Frame rates as function of AOI height[width=2048]

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2048	16.17	16	10	8	10	8	5
1200	25.52	25	18	13	18	13	9
1024	29.00	29	21	16	21	16	10
960	30.52	30	22	17	22	17	11
600	43.20	43	35	27	35	27	18
480	50.15	50	44	33	44	33	22
240	73.95	73	73	66	73	66	44
120	96.94	96	96	96	96	96	88
60	114.79	114	114	114	114	114	114
30	126.43	126	126	126	126	126	126

Table 114: Frame rates as function of AOI height [width=2048]

Pike F-505: AOI frame rates

$$\text{max. frame rate of CCD} = \frac{1}{636\mu s + \text{AOI height} \times 33.10\mu s + (2069 - \text{AOI height}) \times 10.34\mu s}$$

Formula 15: Theoretical max. frame rate of CCD

AOI frame rates with max. BPP = 8192

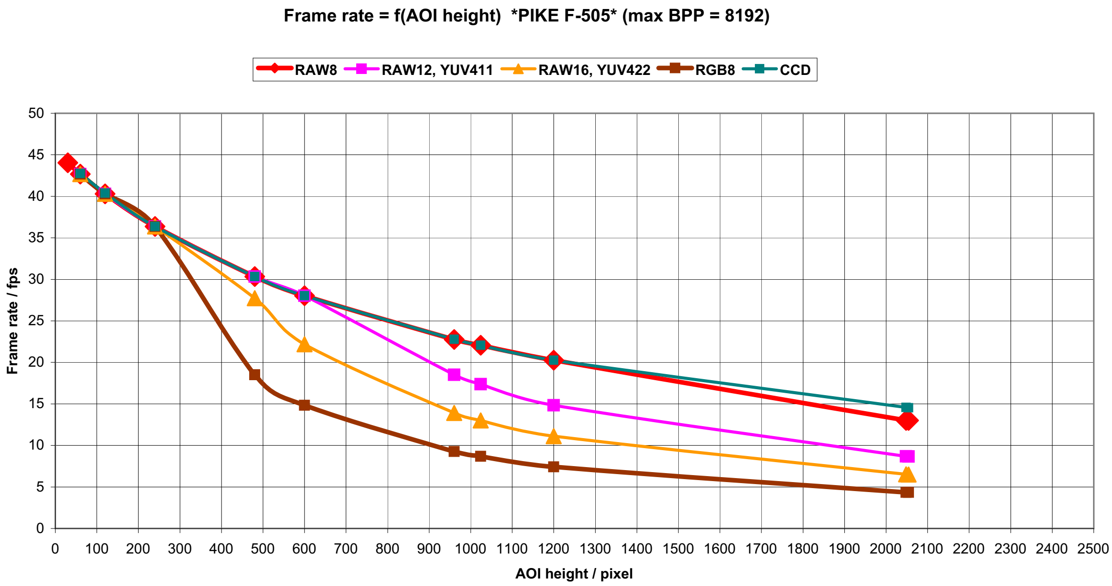


Figure 93: Frame rates as function of AOI height [width=2452] (max BPP = 8192)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2054	14.54	13	9	7	9	7	4
2048	14.57	13	9	7	9	7	4
1200	20.27	20	15	11	15	11	7
1024	22.06	22	17	13	17	13	9
960	22.79	22	18	14	18	14	9
600	28.02	28	28	22	28	22	15
480	30.35	30	30	28	30	28	18
240	36.37	36	36	36	36	36	36
120	40.39	40	40	40	40	40	40
60	42.74	42	42	42	42	42	42
30	44.03	44	44	44	44	44	44

Table 115: Frame rates as function of AOI height [width=2452] (maxBPP=8192)

AOI frame rates with max. BPP = 11000

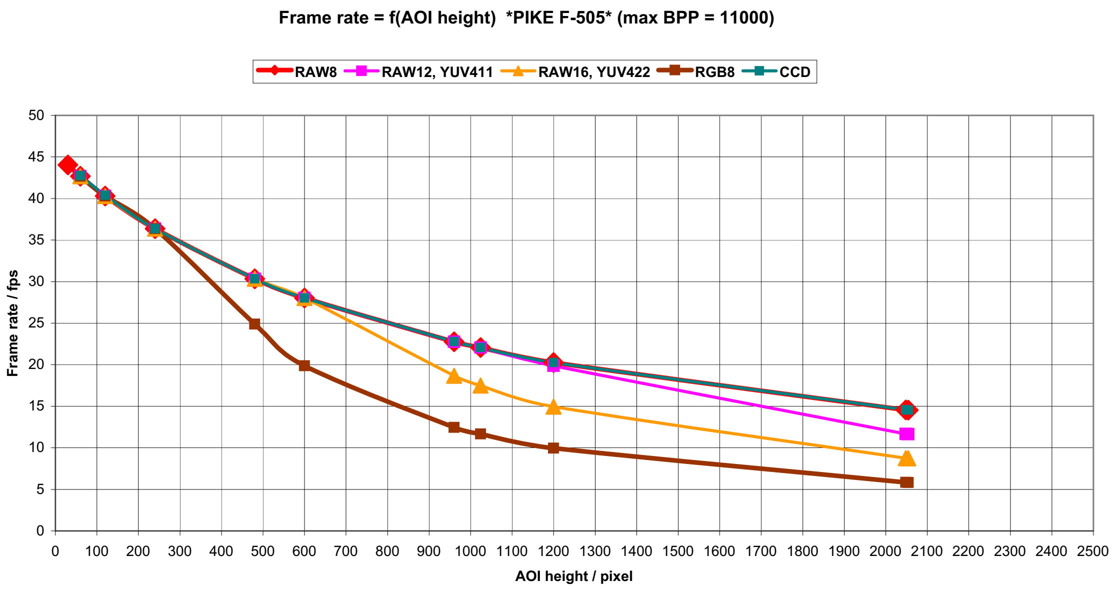


Figure 94: Frame rates as function of AOI height [width=2452] (max BPP = 11000)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2054	14.54	14	12	9	12	9	6
2048	14.57	14	12	9	12	9	6
1200	20.27	20	20	15	20	15	10
1024	22.06	22	22	17	22	17	12
960	22.79	22	22	19	22	19	12
600	28.02	28	28	28	28	28	20
480	30.35	30	30	30	30	30	25
240	36.37	36	36	36	36	36	36
120	40.39	40	40	40	40	40	40
60	42.74	42	42	42	42	42	42
30	44.03	44	44	44	44	44	44

Table 116: Frame rates as function of AOI height [width=2452] (maxBPP=11000)

Note

CCD = theoretical maximum frame rate (in fps) of CCD according to given formula

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

Pike F-1100: AOI frame rates

Pike F-1100: frame rate formula single-tap

All frame rates are valid for AOI top = 0. For AOIs with different positions the values may differ very slightly (first position after decimal point).

$$\text{max. frame rate of CCD}_{\text{single-tap}} = \frac{1}{833.11\mu s + (\text{AOI height} \times 141.41\mu s) + (2721 - \text{AOI height}) \times 12\mu s}$$

Formula 16: Theoretical max. frame rate CCD (maxBPP=8192, single-tap, no sub-sampling)

AOI frame rates maxBPP=8192, single-tap, no sub-sampling

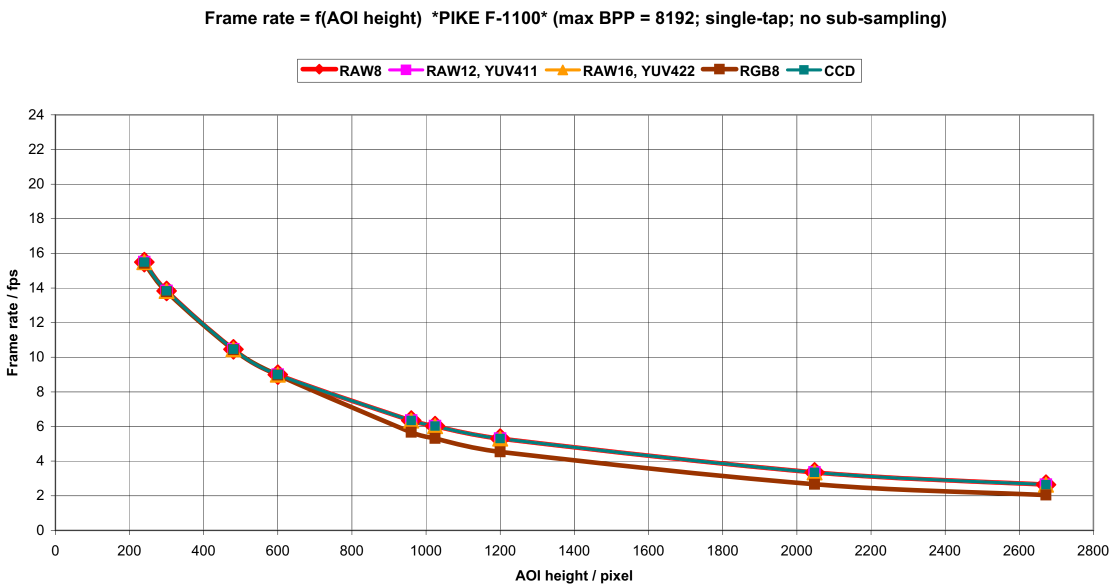


Figure 95: Pike F-1100 [width=4008] (max BPP = 8192, single-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	2.636	2.6	2.6	2.6	2.6	2.6	2.0
2048	3.349	3.3	3.3	3.3	3.3	3.3	2.6
1200	5.297	5.2	5.2	5.2	5.2	5.2	4.5
1024	6.024	6.0	6.0	6.0	6.0	6.0	5.3
960	6.340	6.3	6.3	6.3	6.3	6.3	5.6
600	8.998	8.9	8.9	8.9	8.9	8.9	8.9
480	10.46	10.4	10.4	10.4	10.4	10.4	10.4
300	13.82	13.8	13.8	13.8	13.7	13.7	13.7
240	15.49	15.4	15.4	15.4	15.4	15.4	15.4

Table 117: Pike F-1100 [width=4008] (max BPP = 8192, single-tap, no sub-sampling)

AOI frame rates maxBPP=8192, single-tap, sub-sampling

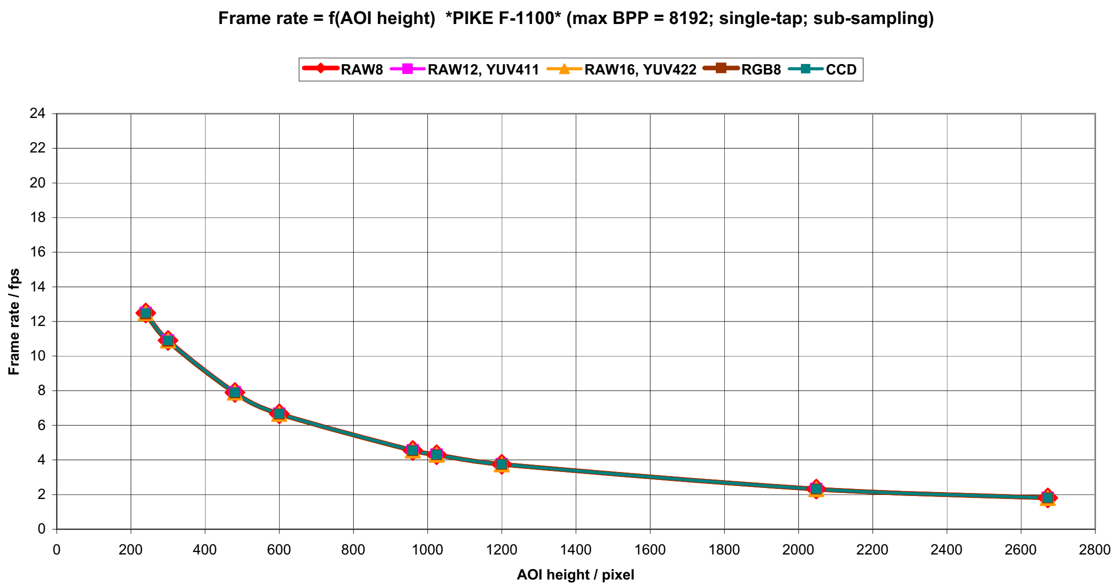


Figure 96: Pike F-1100 [width=4008] (maxBPP=8192, single-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	1.811	1.8	1.8	1.8	1.8	1.8	1.8
2048	2.320	2.3	2.3	2.3	2.3	2.3	2.3
1200	3.753	3.7	3.7	3.7	3.7	3.7	3.7
1024	4.305	4.3	4.3	4.3	4.2	4.2	4.2
960	4.548	4.5	4.5	4.5	4.5	4.5	4.5
600	6.668	6.6	6.6	6.6	6.6	6.6	6.6
480	7.895	7.8	7.8	7.8	7.8	7.8	7.8
300	10.90	10.9	10.9	10.9	10.8	10.8	10.8
240	12.48	12.4	12.4	12.4	12.4	12.4	12.4

Table 118: Pike F-1100 [width=4008] (maxBPP=8192, single-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD maxBPP=8192 according to IIDC V1.31

Pike F-1100: frame rate formula dual-tap

All frame rates are valid for AOI top = 0. For AOIs with different positions the values may differ very slightly (first position after decimal point).

$$\text{max. frame rate of CCD}_{\text{dual-tap}} = \frac{1}{518.13\mu s + (\text{AOI height} \times 74.85\mu s) + (2721 - \text{AOI height}) \times 12\mu s}$$

Formula 17: Theoretical max. frame rate of CCD (maxBPP=8192, dual-tap, no sub-sampling)

AOI frame rates maxBPP=8192, dual-tap, no sub-sampling

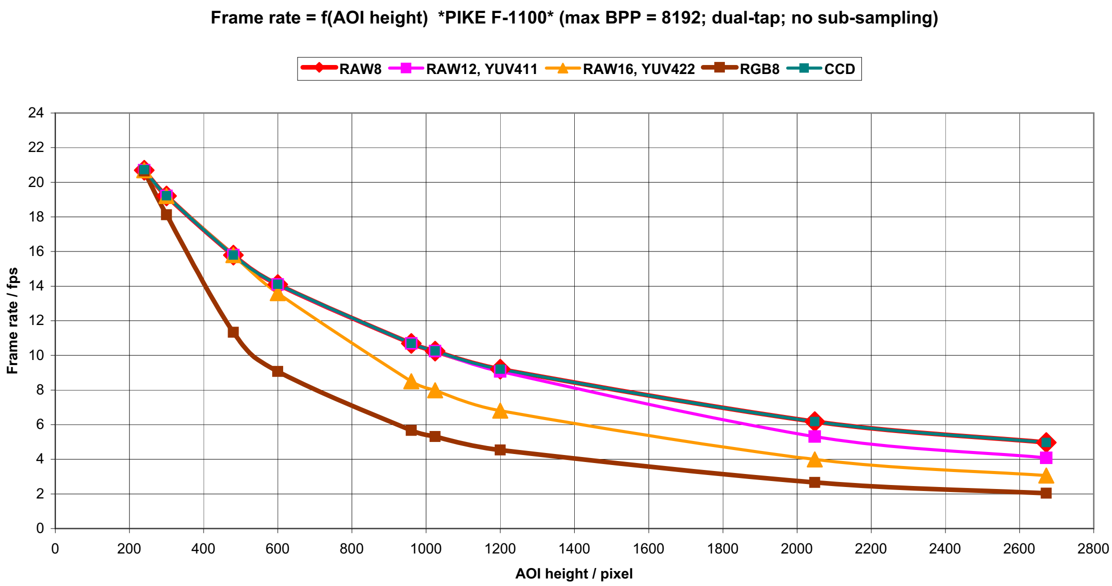


Figure 97: Pike F-1100 [width=4008] (maxBPP=8192, dual-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	4.972	4.9	4.0	3.0	4.0	3.0	2.0
2048	6.177	6.1	5.3	3.9	5.3	3.9	2.6
1200	9.208	9.2	9.0	6.8	9.0	6.8	4.5
1024	10.25	10.2	10.2	7.9	10.2	7.9	5.3
960	10.69	10.6	10.6	8.5	10.6	7.9	5.6
600	14.10	14.0	14.0	13.5	14.0	13.5	9.0
480	15.78	15.7	15.7	15.7	15.7	15.7	11.3
300	19.22	19.2	19.2	19.2	19.1	19.1	18.1
240	20.72	20.6	20.6	20.6	20.6	20.6	20.6

Table 119: Pike F-1100 [width=4008] (maxBPP=8192, dual-tap, no sub-sampling)

AOI frame rates maxBPP=8192, dual-tap, sub-sampling

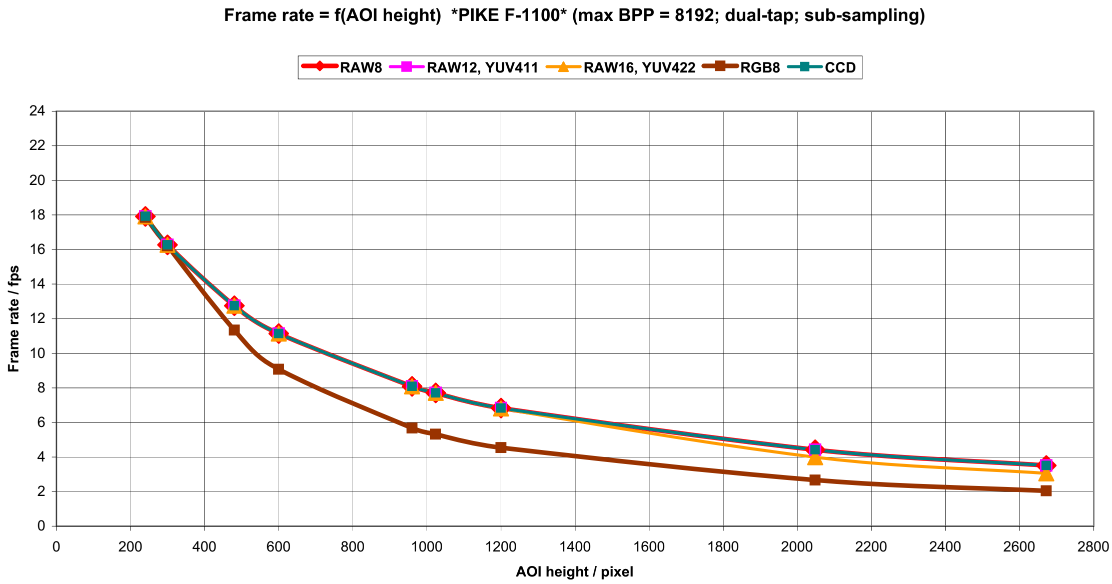


Figure 98: Pike F-1100 [width=4008] (maxBPP=8192, dual-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	3.507	3.5	3.5	3.0	3.5	3.0	2.0
2048	4.419	4.4	4.4	3.9	4.4	3.9	2.6
1200	6.835	6.8	6.8	6.8	6.8	6.8	4.5
1024	7.709	7.7	7.7	7.7	7.6	7.6	5.3
960	8.085	8.0	8.0	8.0	8.0	8.0	5.6
600	11.14	11.1	11.1	11.1	11.1	11.1	9.0
480	12.75	12.7	12.7	12.7	12.7	12.7	11.3
300	16.27	16.2	16.2	16.2	16.2	16.2	16.2
240	17.92	17.9	17.9	17.9	17.8	17.8	17.8

Table 120: Pike F-1100 [width=4008] (maxBPP=8192, dual-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD maxBPP=8192 according to IIDC V1.31

AOI frame rates maxBPP=11000, single-tap, no sub-sampling

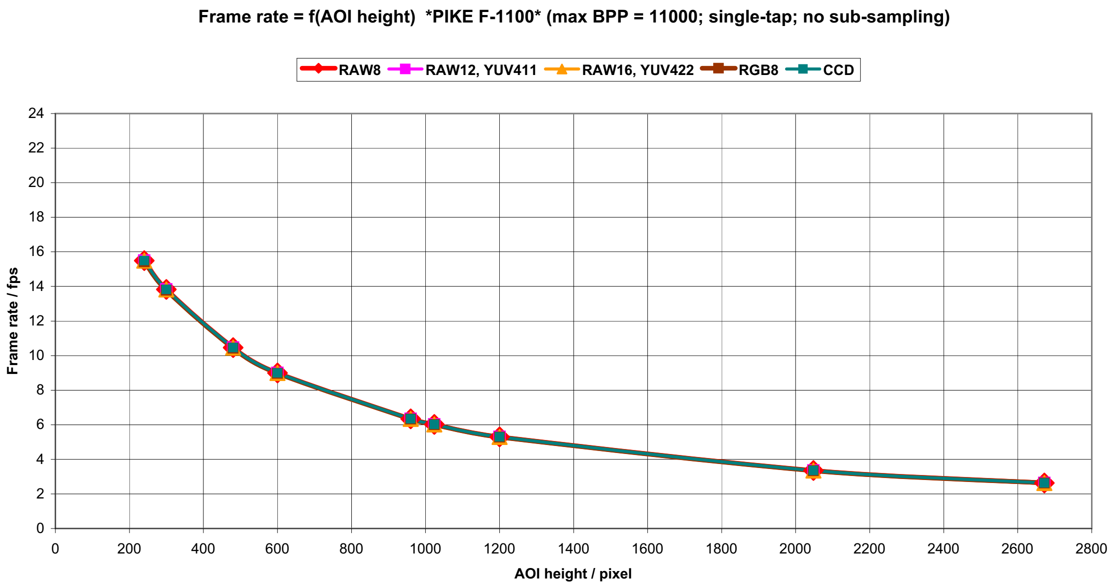


Figure 99: Pike F-1100 [width=4008] (maxBPP=11000, single-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	2.636	2.6	2.6	2.6	2.6	2.6	2.6
2048	3.349	3.3	3.3	3.3	3.3	3.3	3.3
1200	5.297	5.2	5.2	5.2	5.2	5.2	5.2
1024	6.024	6.0	6.0	6.0	6.0	6.0	6.0
960	6.340	6.3	6.3	6.3	6.3	6.3	6.3
600	8.998	8.9	8.9	8.9	8.9	8.9	8.9
480	10.46	10.4	10.4	10.4	10.4	10.4	10.4
300	13.82	13.8	13.8	13.8	13.7	13.7	13.7
240	15.49	15.4	15.4	15.4	15.4	15.4	15.4

Figure 100: Pike F-1100 [width=4008] (maxBPP=11000, single-tap, no sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

AOI frame rates maxBPP=11000, single-tap, sub-sampling

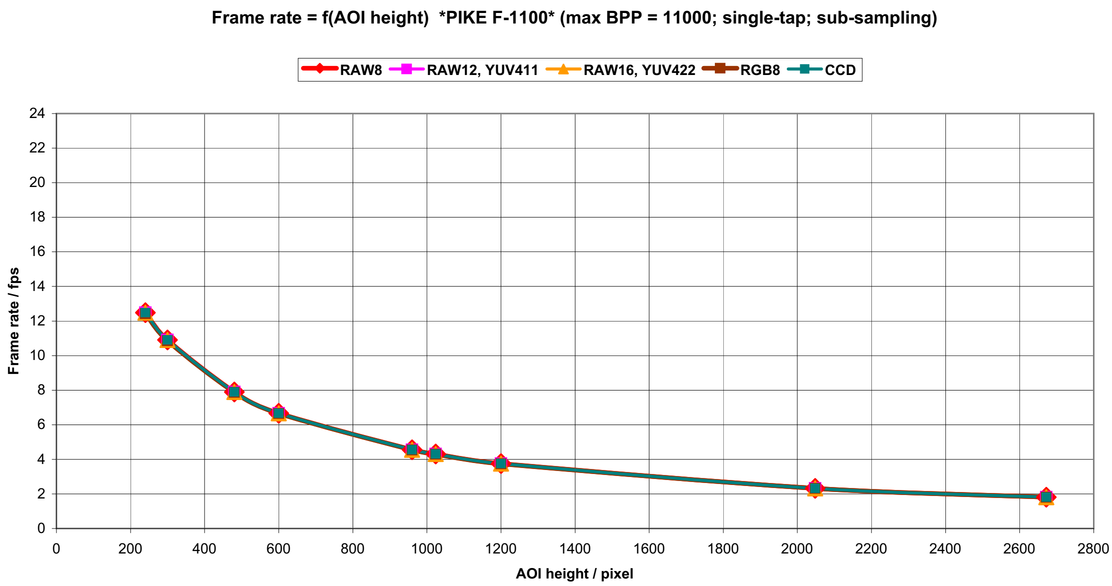


Figure 101: Pike F-1100 [width=4008] (maxBPP=11000, single-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	1.811	1.8	1.8	1.8	1.8	1.8	1.8
2048	2.320	2.3	2.3	2.3	2.3	2.3	2.3
1200	3.753	3.7	3.7	3.7	3.7	3.7	3.7
1024	4.305	4.3	4.3	4.3	4.2	4.2	4.2
960	4.548	4.5	4.5	4.5	4.5	4.5	4.5
600	6.687	6.6	6.6	6.6	6.6	6.6	6.6
480	7.895	7.8	7.8	7.8	7.8	7.8	7.8
300	10.90	10.9	10.9	10.9	10.8	10.8	10.8
240	12.48	12.4	12.4	12.4	12.4	12.4	12.4

Table 121: Pike F-1100 [width=4008] (maxBPP=11000, single-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

AOI frame rates maxBPP=11000, dual-tap, no sub-sampling

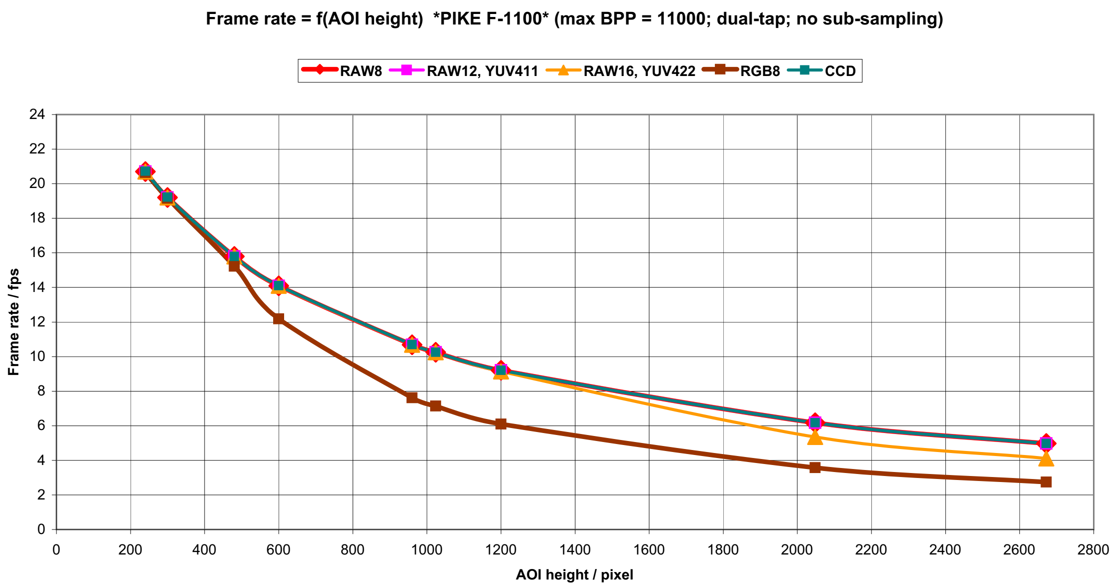


Figure 102: Pike F-1100 [width=4008] (max BPP=11000, dual-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	4.972	4.9	4.9	4.1	4.9	4.1	2.7
2048	6.177	6.1	6.1	5.3	6.1	5.3	3.5
1200	9.208	9.2	9.2	9.1	9.1	9.1	6.0
1024	10.25	10.2	10.2	10.2	10.2	10.2	7.1
960	10.69	10.6	10.6	10.6	10.6	10.6	7.6
600	14.10	14.0	14.0	14.0	14.0	14.0	12.1
480	15.78	15.7	15.7	15.7	15.7	15.7	15.2
300	19.22	19.2	19.2	19.2	19.1	19.1	19.1
240	20.72	20.6	20.6	20.6	20.6	20.6	20.6

Table 122: Pike F-1100 [width=4008] (maxBPP=11000, dual-tap, no sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

AOI frame rates maxBPP=11000, dual-tap, sub-sampling

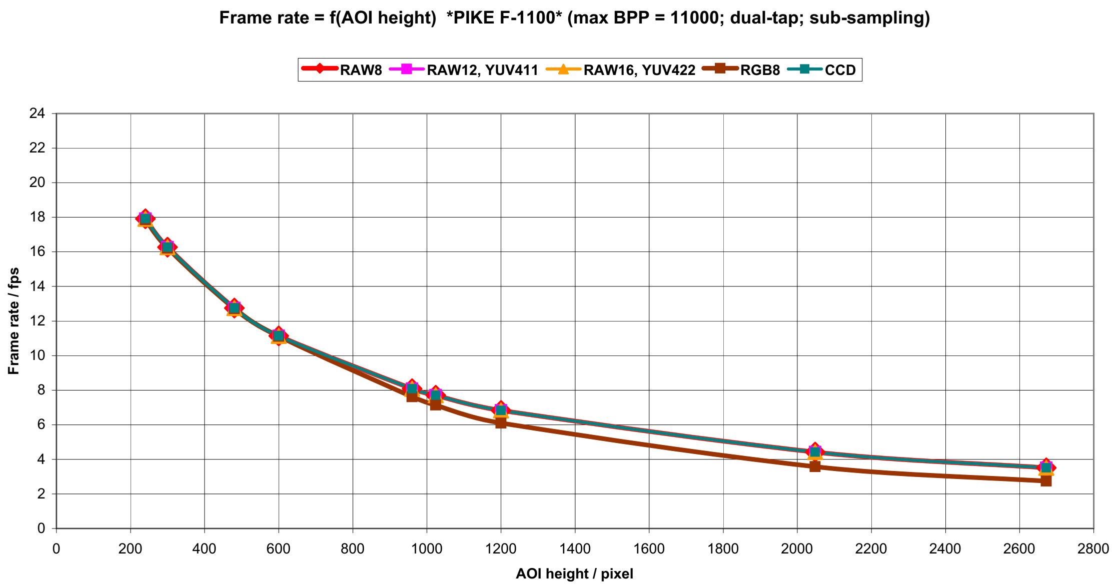


Figure 103: Pike F-1100 [width=4008] (maxBPP=11000, dual-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
2672	3.507	3.5	3.5	3.5	3.5	3.5	2.7
2048	4.419	4.4	4.4	4.4	4.4	4.4	3.5
1200	6.835	6.8	6.8	6.8	6.8	6.8	6.0
1024	7.709	7.7	7.7	7.7	7.6	7.6	7.1
960	8.085	8.0	8.0	8.0	8.0	8.0	7.6
600	11.14	11.1	11.1	11.1	11.1	11.1	11.1
480	12.75	12.7	12.7	12.7	12.7	12.7	12.7
300	16.27	16.2	16.2	16.2	16.2	16.2	16.2
240	17.92	17.9	17.9	17.9	17.8	17.8	17.8

Table 123: Pike F-1100 [width=4008] (maxBPP=11000, dual-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

Pike F-1600: AOI frame rates

Pike F-1600: frame rate formula single-tap

All frame rates are valid for AOI top = 0. For AOIs with different positions the values may differ very slightly (first position after decimal point).

$$\text{max. frame rate of CCD}_{\text{single-tap}} = \frac{1}{1778.12\mu s + \text{AOI height} \times 177.05\mu s + (3324 - \text{AOI height}) \times 13.64\mu s}$$

Formula 18: Theoretical max. frame rate CCD (maxBPP=8192, single-tap, no sub-sampling)

AOI frame rates maxBPP=8192, single-tap, no sub-sampling

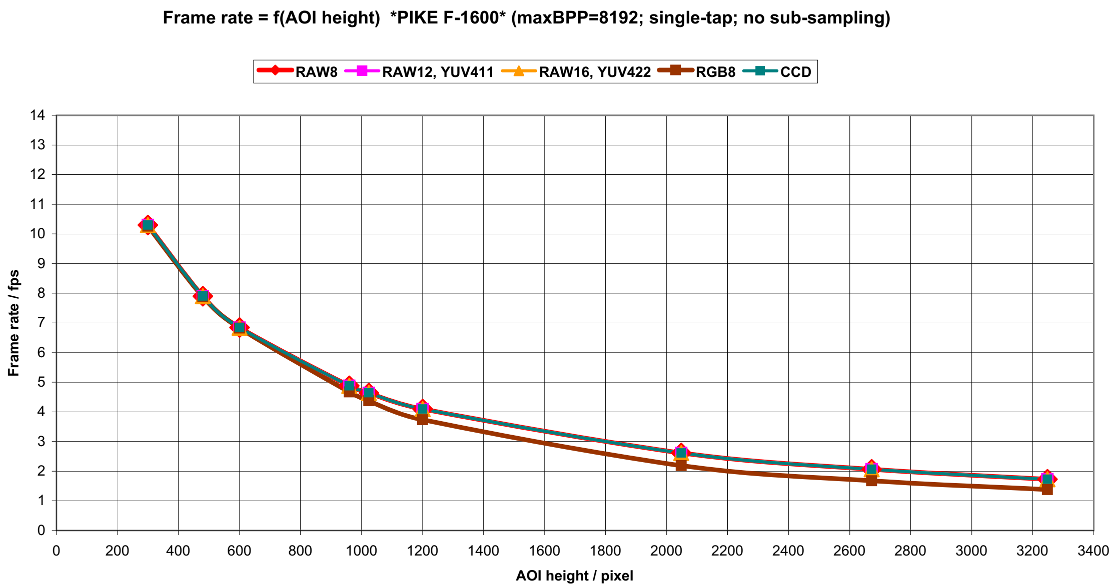


Figure 104: Pike F-1600 [width=4872] (max BPP = 8192, single-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	1.727	1.7	1.7	1.7	1.7	1.7	1.3
2672	2.063	2.0	2.0	2.0	2.0	2.0	1.6
2048	2.612	2.6	2.6	2.6	2.6	2.6	2.1
1200	4.095	4.0	4.0	4.0	4.0	4.0	3.7
1024	4.641	4.6	4.6	4.6	4.6	4.6	4.3
960	4.878	4.8	4.8	4.8	4.8	4.8	4.6
600	6.842	6.8	6.8	6.8	6.8	6.8	6.8
480	7.902	7.9	7.9	7.9	7.8	7.8	7.8
300	10.29	10.2	10.2	10.2	10.2	10.2	10.2

Table 124: Pike F-1600 [width=4872] (maxBPP=8192, single-tap, no sub-sampling)

AOI frame rates maxBPP=8192, single-tap, sub-sampling

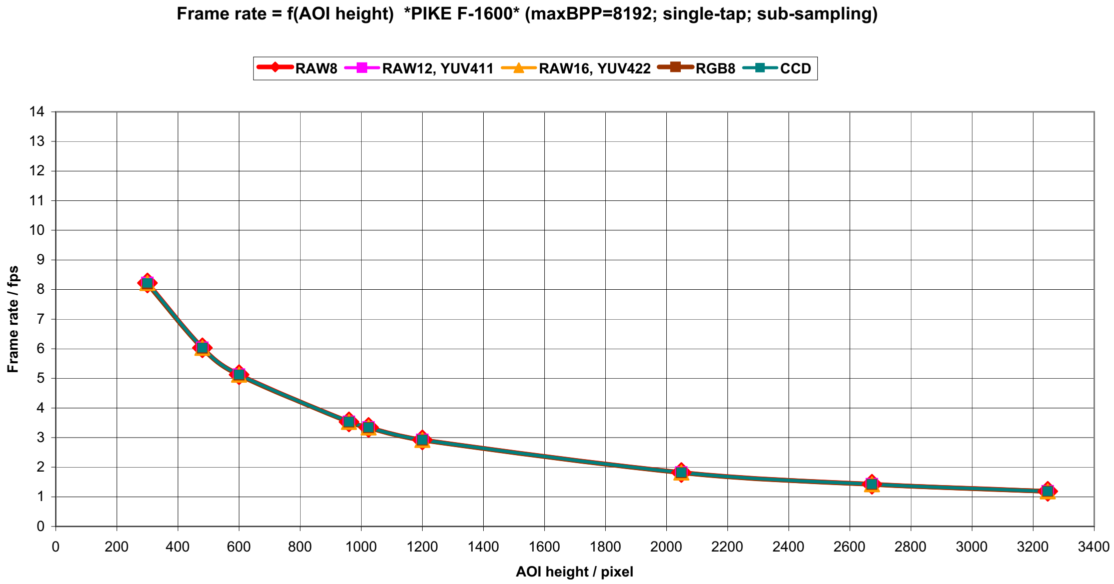


Figure 105: Pike F-1600 [width=4872] (max BPP = 8192, single-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	1.184	1.1	1.1	1.1	1.1	1.1	1.1
2672	1.422	1.4	1.4	1.4	1.4	1.4	1.4
2048	1.817	1.8	1.8	1.8	1.8	1.8	1.8
1200	2.921	2.9	2.9	2.9	2.9	2.9	2.9
1024	3.343	3.3	3.3	3.3	3.3	3.3	3.3
960	3.528	3.5	3.5	3.5	3.5	3.5	3.5
600	5.123	5.1	5.1	5.1	5.1	5.1	5.1
480	6.033	6.03	6.03	6.03	6.01	6.01	6.01
300	8.221	8.22	8.22	8.22	8.18	8.18	8.18

Table 125: Pike F-1600 [width=4872] (maxBPP=8192, single-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD maxBPP=8192 according to IIDC V1.31

Pike F-1600: frame rate formula dual-tap

All frame rates are valid for AOI top = 0. For AOIs with different positions the values may differ very slightly (first position after decimal point).

$$\text{max. frame rate of CCD}_{\text{dual-tap}} = \frac{1}{1534\mu s + \text{AOI height} \times 95.67\mu s + (3324 - \text{AOI height}) \times 13.64\mu s}$$

Formula 19: Theoretical max. frame rate of CCD (maxBPP=8192, dual-tap, no sub-sampling)

AOI frame rates maxBPP=8192, dual-tap, no sub-sampling

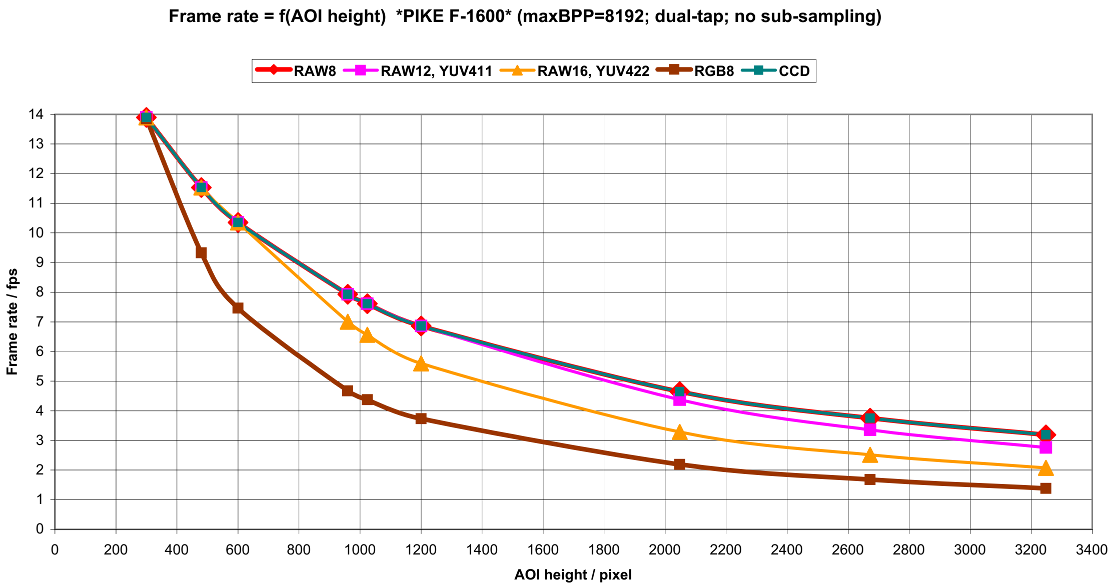


Figure 106: Pike F-1600 [width=4872] (max BPP = 8192, dual-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	3.186	3.18	2.76	2.07	2.76	2.07	1.38
2672	3.751	3.75	3.35	2.51	3.35	2.51	1.67
2048	4.643	4.64	4.37	3.28	4.37	3.28	2.18
1200	6.858	6.85	6.85	5.60	6.85	5.60	3.73
1024	7.612	7.61	7.61	6.56	7.60	6.56	4.37
960	7.929	7.92	7.92	7.00	7.91	7.00	4.66
600	10.35	10.3	10.3	10.3	10.3	10.3	7.46
480	11.52	11.5	11.5	11.5	11.5	11.5	9.32
300	13.89	13.8	13.8	13.8	13.8	13.8	13.8

Table 126: Pike F-1600 [width=4872] (maxBPP=8192, dual-tap, no sub-sampling)

AOI frame rates maxBPP=8192, dual-tap, sub-sampling

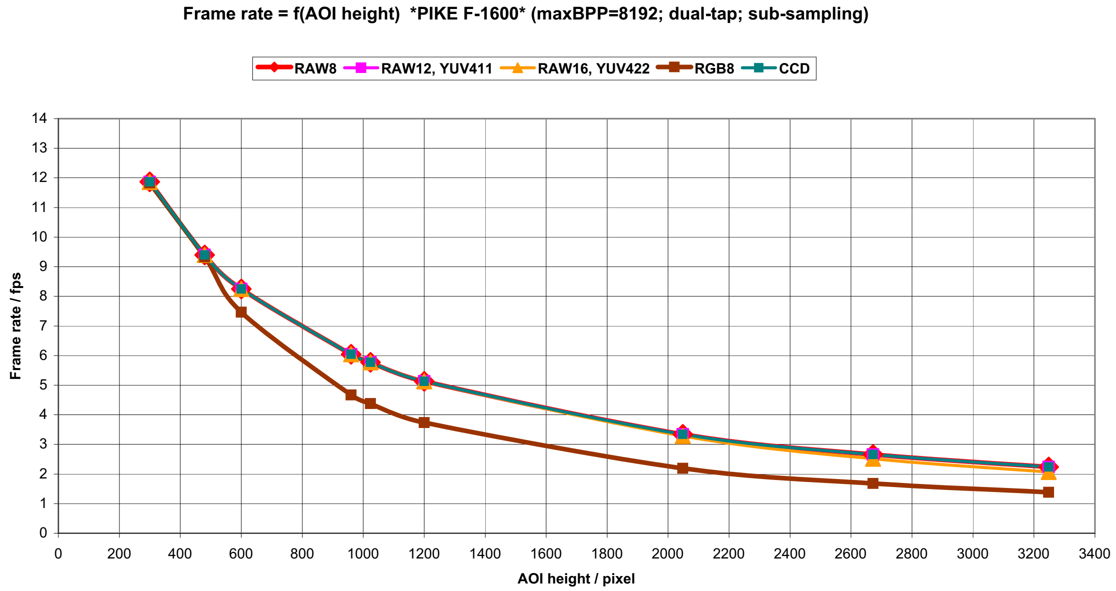


Figure 107: Pike F-1600 [width=4872] (max BPP = 8192, dual-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	2.237	2.23	2.23	2.07	2.23	2.07	1.38
2672	2.658	2.65	2.65	2.51	2.65	2.51	1.67
2048	3.340	3.34	3.34	3.28	3.33	3.28	2.18
1200	5.127	5.12	5.12	5.12	5.12	5.12	3.73
1024	5.768	5.76	5.76	5.76	5.76	5.76	4.37
960	6.042	6.04	6.04	6.04	6.03	6.03	4.66
600	8.251	8.25	8.25	8.25	8.23	8.23	7.46
480	9.396	9.39	9.39	9.39	9.37	9.37	9.32
300	11.86	11.8	11.8	11.8	11.8	11.8	11.8

Table 127: Pike F-1600 [width=4872] (maxBPP=8192, dual-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD maxBPP=8192 according to IIDC V1.31

AOI frame rates maxBPP=16000, single-tap, no sub-sampling

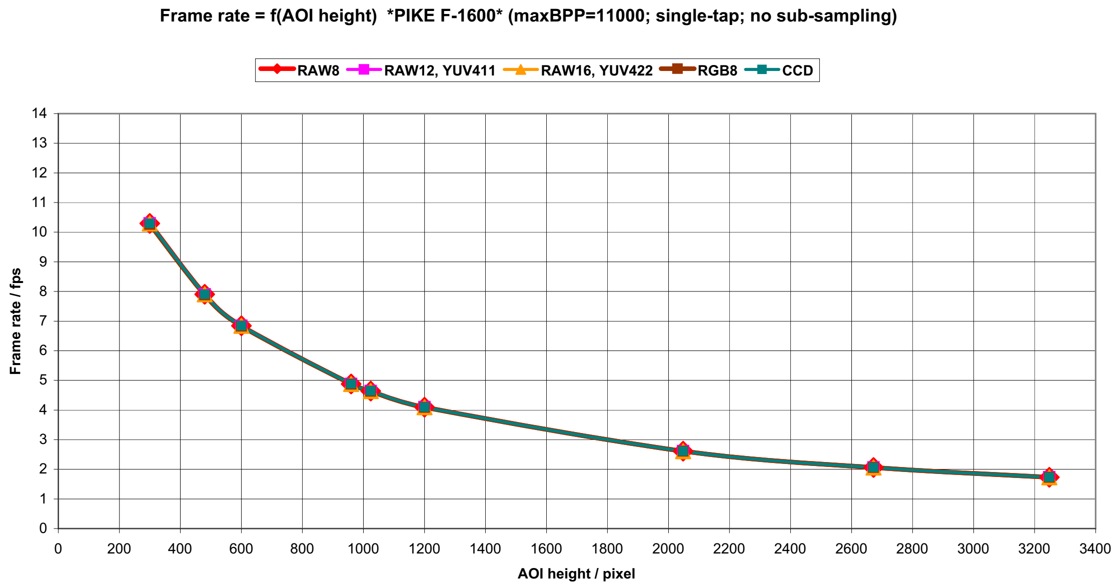


Figure 108: Pike F-1600 [width=4872] (max BPP = 11000, single-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	1.727	1.72	1.72	1.72	1.72	1.72	1.72
2672	2.063	2.06	2.06	2.06	2.06	2.06	2.06
2048	2.612	2.61	2.61	2.61	2.61	2.61	2.61
1200	4.095	4.09	4.09	4.09	4.08	4.08	4.08
1024	4.641	4.64	4.64	4.64	4.63	4.63	4.63
960	4.878	4.87	4.87	4.87	4.87	4.87	4.87
600	6.842	6.84	6.84	6.84	6.82	6.82	6.82
480	7.902	7.90	7.90	7.90	7.88	7.88	7.88
300	10.29	10.2	10.2	10.2	10.2	10.2	10.2

Table 128: Pike F-1600 [width=4872] (maxBPP=11000, single-tap, no sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

AOI frame rates maxBPP=11000, single-tap, sub-sampling

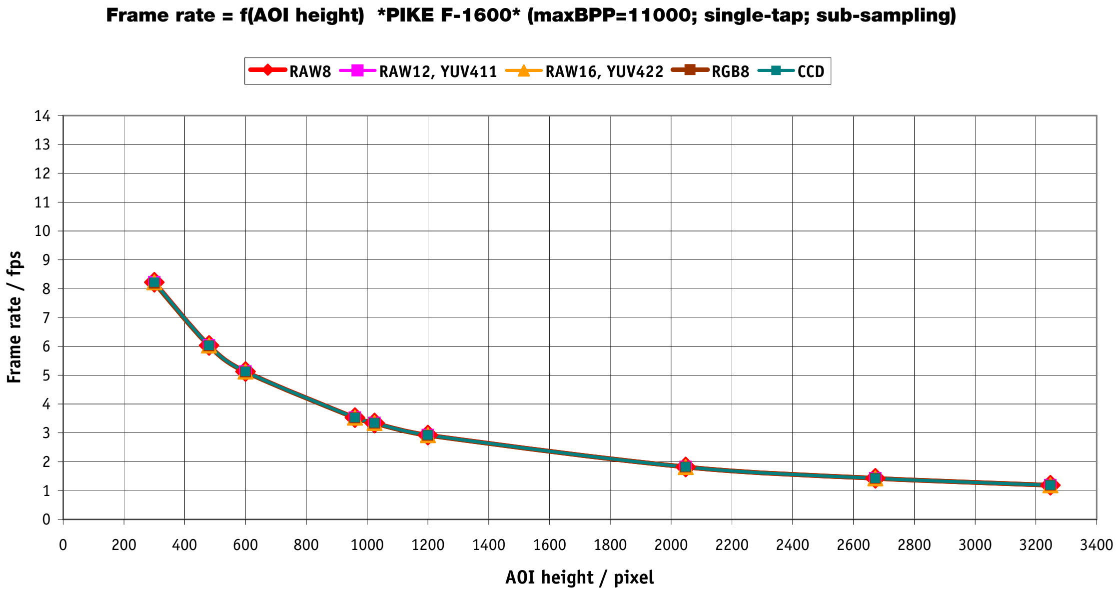


Figure 109: Pike F-1600 [width=4872] (max BPP = 11000, single-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	1.184	1.18	1.18	1.18	1.18	1.18	1.18
2672	1.422	1.42	1.42	1.42	1.42	1.42	1.42
2048	1.817	1.81	1.81	1.81	1.81	1.81	1.81
1200	2.921	2.92	2.92	2.92	2.91	2.91	2.91
1024	3.343	3.34	3.34	3.34	3.33	3.33	3.33
960	3.528	3.52	3.52	3.52	3.52	3.52	3.52
600	5.123	5.12	5.12	5.12	5.11	5.11	5.11
480	6.033	6.03	6.03	6.03	6.01	6.01	6.01
300	8.221	8.22	8.22	8.22	8.18	8.18	8.18

Table 129: Pike F-1600 [width=4872] (maxBPP=11000, single-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

AOI frame rates maxBPP=11000, dual-tap, no sub-sampling

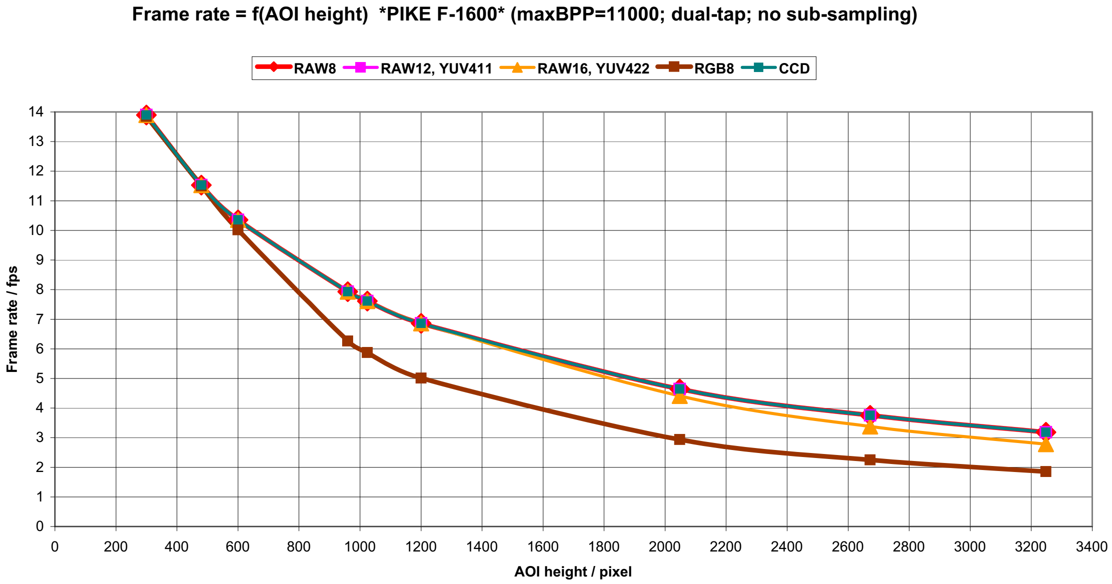


Figure 110: Pike F-1600 [width=4872] (max BPP = 11000, dual-tap, no sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	3.186	3.18	3.18	2.77	3.18	2.77	1.85
2672	3.751	3.75	3.75	3.37	3.74	3.37	2.25
2048	4.643	4.64	4.64	4.40	4.63	4.40	2.93
1200	6.858	6.85	6.85	6.85	6.85	6.85	5.01
1024	7.612	7.61	7.61	7.61	7.60	7.60	5.87
960	7.929	7.92	7.92	7.92	7.91	7.91	6.26
600	10.35	10.3	10.3	10.3	10.3	10.3	10.0
480	11.52	11.5	11.5	11.5	11.5	11.5	11.5
300	13.89	13.8	13.8	13.8	13.8	13.8	13.8

Table 130: Pike F-1600 [width=4872] (maxBPP=11000, dual-tap, no sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

AOI frame rates maxBPP=11000, dual-tap, sub-sampling

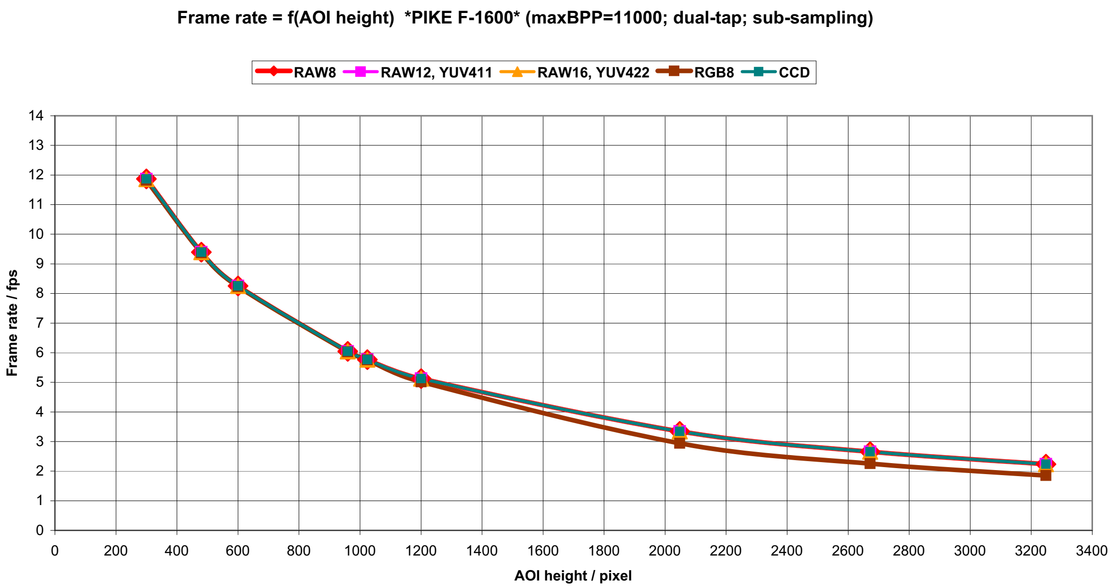


Figure 111: Pike F-1600 [width=4872] (max BPP = 11000, dual-tap, sub-sampling)

AOI height	CCD	RAW8	RAW12	RAW16	YUV411	YUV422	RGB8
3248	2.237	2.23	2.23	2.23	2.23	2.23	1.85
2672	2.658	2.65	2.65	2.65	2.65	2.65	2.25
2048	3.340	3.34	3.34	3.34	3.33	3.33	2.93
1200	5.127	5.12	5.12	5.12	5.12	5.12	5.01
1024	5.768	5.76	5.76	5.76	5.76	5.76	5.76
960	6.042	6.04	6.04	6.04	6.03	6.03	6.03
600	8.251	8.25	8.25	8.25	8.23	8.23	8.23
480	9.396	9.39	9.39	9.39	9.37	9.37	9.37
300	11.86	11.8	11.8	11.8	11.8	11.8	11.8

Table 131: Pike F-1600 [width=4872] (maxBPP=11000, dual-tap, sub-sampling)

Note

CCD = theoretical maximum frame rate (in fps) of CCD

maxBPP: for explanation and configuration see Maximum ISO packet size on page 315

How does bandwidth affect the frame rate?

In some modes the IEEE1394b bus limits the attainable frame rate. According to the 1394b specification on isochronous transfer, the largest data payload size of 8192 bytes per 125 µs cycle is possible with bandwidth of 800 Mbit/s. In addition, there is a limitation, only a maximum number of 65535 (2^{16} -1) packets per frame are allowed.

The following formula establishes the relationship between the required Byte_Per_Packet size and certain variables for the image. It is valid only for Format_7.

$$\text{BYTE\_PER\_PACKET} = \text{frame rate}[1/s] \times \text{AOI\_WIDTH} \times \text{AOI\_HEIGHT} \times \text{ByteDepth [byte]} \times 125\ [\mu s]$$

Formula 20: Byte_per_Packet calculation (only Format_7)

If the value for BYTE_PER_PACKET is greater than 8192 (the maximum data payload), the sought-after frame rate cannot be attained. The attainable frame rate can be calculated using this formula:

(Provision: BYTE_PER_PACKET is divisible by 4):

$$\text{frame rate} \approx \frac{\text{BYTE\_PER\_PACKET [byte]}}{\text{AOI\_WIDTH} \times \text{AOI\_HEIGHT} \times \text{ByteDepth [byte]} \times 125\ [\mu s]}$$

Formula 21: Maximum frame rate calculation

ByteDepth based on the following values:

Mode	bit/pixel	byte per pixel
Mono8, Raw8	8	1
Mono16, Raw16	16	2
YUV4:2:2	16	2
YUV4:1:1	12	1.5
RGB8	24	3

Table 132: ByteDepth

Example formula for the monochrome camera

Mono16, 1392 × 1040, 30 fps desired

$$\text{BYTE\_PER\_PACKET} = 30\ 1/\text{s} \times 1392 \times 1040 \times 2\ \text{byte} \times 125\mu\text{s} = 10856\ \text{byte} > 8192\ \text{byte}$$

$$\Rightarrow \text{frame rate}_{\text{reachable}} \approx \frac{8192\ \text{byte}}{1392 \times 1040 \times 2\ \text{byte} \times 125\mu\text{s}} = 22.64\ 1/\text{s}$$

Formula 22: Example maximum frame rate calculation

Test images

Loading test images

FirePackage	Direct FirePackage	Fire4Linux
1. Start SmartView. 2. Click the Edit settings button.  3. Click Adv1 tab. 4. In combo box Test images choose Image 1 or another test image.	1. Start SmartView for WDM. 2. In Camera menu click Settings. 3. Click Adv1 tab. 4. In combo box Test images choose Image 1 or another test image.	1. Start cc1394 viewer. 2. In Adjustments menu click on Picture Control. 3. Click Main tab. 4. Activate Test image check box on. 5. In combo box Test images choose Image 1 or another test image.

Table 133: Loading test images in different viewers

Test images for monochrome cameras

The monochrome cameras have two test images that look the same. Both images show a gray bar running diagonally (mirrored at the middle axis).

- Image 1 is static.
- Image 2 moves upwards by 1 pixel/frame.

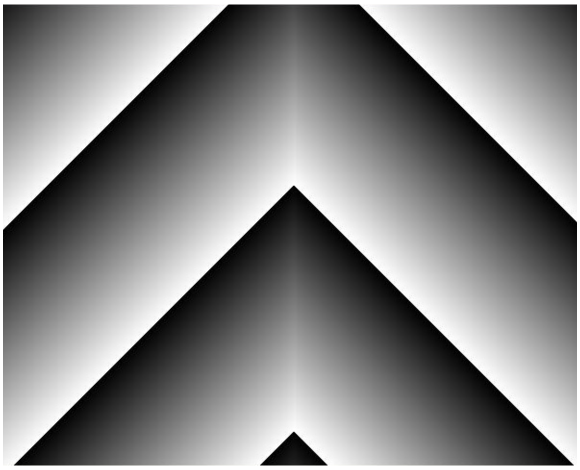


Figure 112: Gray bar test image

Test images for color cameras

The color cameras have 1 test image:

YUV4:2:2 mode

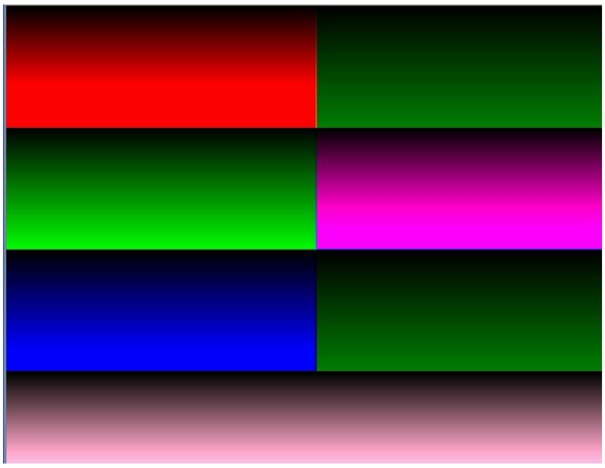


Figure 113: Color test image

Mono8 (raw data)

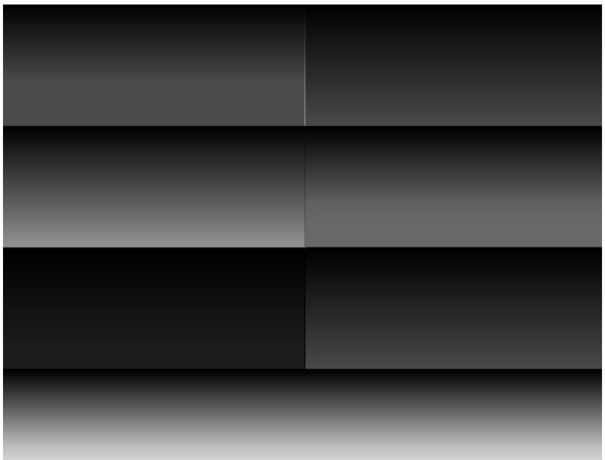


Figure 114: Bayer-coded test image

The color camera outputs Bayer-coded raw data in Mono8 instead of (as described in IIDC V1.31) a real Y signal.

Note

The first pixel of the image is always the red pixel from the sensor. (Mirror must be switched off.)

Configuration of the camera

All camera settings are made by writing specific values into the corresponding registers.

This applies to:

- values for general operating states such as video formats and modes, exposure times, etc.
- extended features of the camera that are turned on and off and controlled via corresponding registers (so-called advanced registers).

Camera_Status_Register

The interoperability of cameras from different manufacturers is ensured by IIDC, formerly DCAM (Digital Camera Specification), published by the IEEE1394 Trade Association.

IIDC is primarily concerned with setting memory addresses (e.g. CSR: Camera_Status_Register) and their meaning.

In principle all addresses in IEEE1394 networks are 64 bits long.

The first 10 bits describe the Bus_Id, the next 6 bits the Node_Id.

Of the subsequent 48 bits, the first 16 bits are always FFFFh, leaving the description for the Camera_Status_Register in the last 32 bits.

If in the following, mention is made of a CSR F0F00600h, this means in full:

Bus_Id, Node_Id, FFFF F0F00600h

Writing and reading to and from the register can be done with programs such as `FireView` or by other programs developed using an API library (e.g. `FirePackage`).

Every register is 32 bit (big endian) and implemented as follows (MSB = Most Significant Bit; LSB = Least Significant Bit):

Far left

Bit 0	Bit 1	Bit 2	...	Bit 30	Bit 31
MSB					LSB

Table 134: 32-bit register

Example

This requires, for example, that to enable `ISO_Enabled mode` (see ISO_Enable / free-run on page 188), (bit 0 in register 614h), the value 80000000 h must be written in the corresponding register.

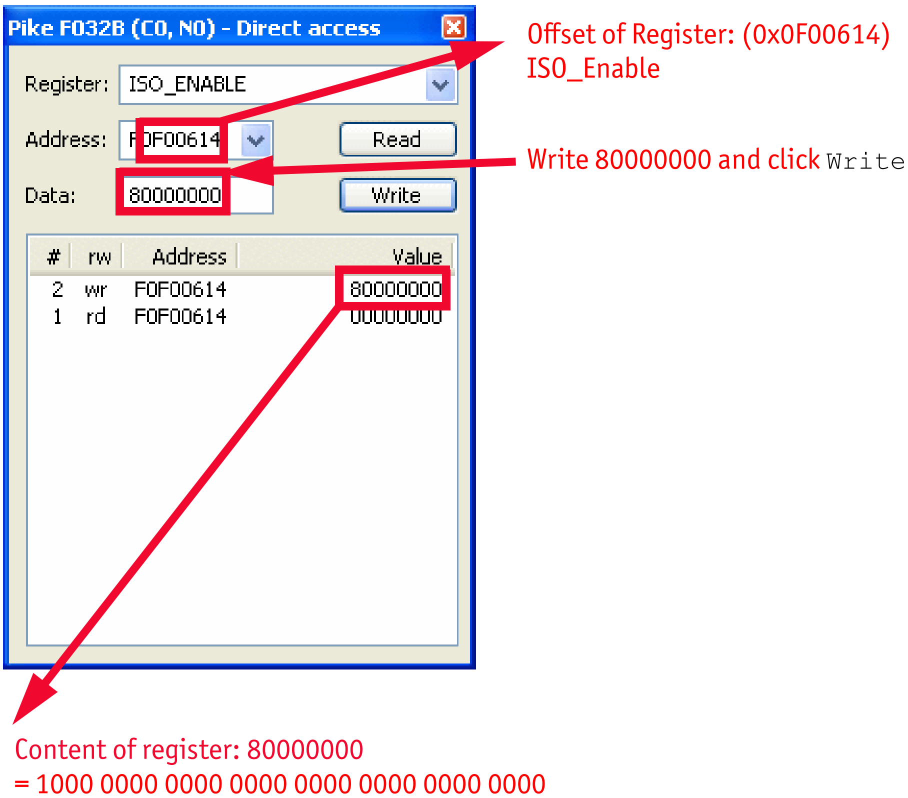


Figure 115: Enabling ISO_Enable

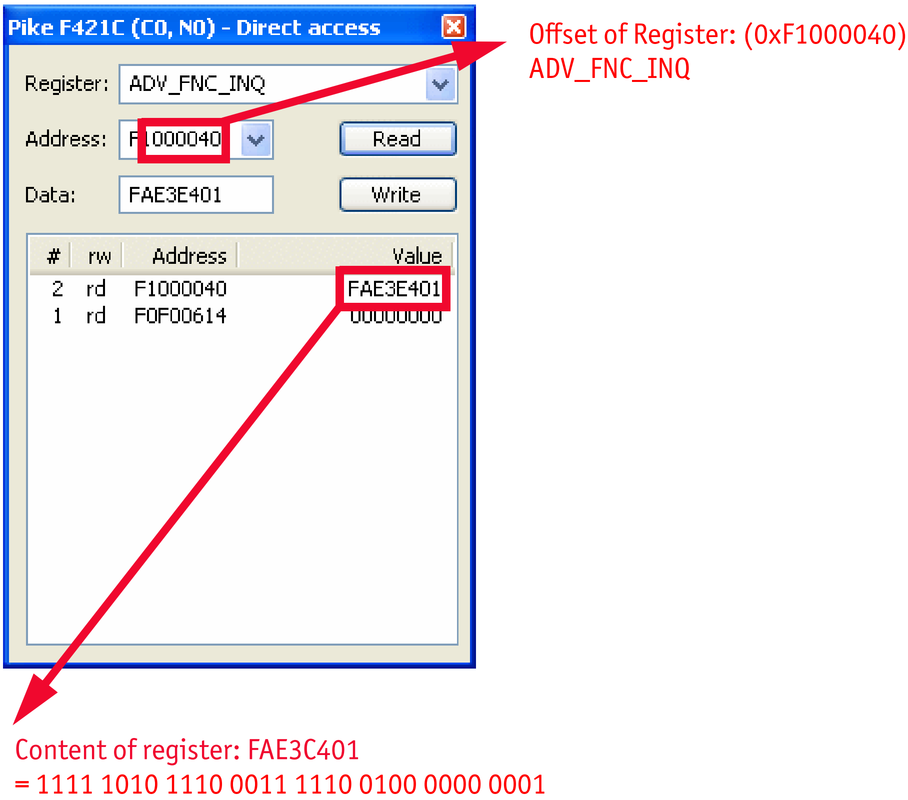


Table 135: Configuring the camera (Pike F-421C)

	MaxResolution	TimeBase	ExtdShutter	Testimage			VersionInfo		Look-up tables	Shading	DeferredTrans				Trigger Delay	Misc. features
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1	1	1	1	1	0	1	0	1	1	1	0	0	0	1	1

	SoftReset	High SNR	ColorCorr			UserProfiles										GP_Buffer
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1

Table 136: Configuring the camera: registers

Sample program

The following sample code in C/C++ shows how the register is set for video mode/format, trigger mode etc. using the `FireGrab` and `FireStack API`.

Example FireGrab

```
…
// Set Videoformat
 if(Result==FCE_NOERROR)
 Result= Camera.SetParameter(FGP_IMAGEFORMAT,MAKEIMAGEFORMAT(RES_640_480, CM_Y8, FR_15));

 // Set external Trigger
 if(Result==FCE_NOERROR)
 Result= Camera.SetParameter(FGP_TRIGGER,MAKETRIGGER(1,0,0,0,0));

 // Start DMA logic
 if(Result==FCE_NOERROR)
  Result=Camera.OpenCapture();

 // Start image device
 if(Result==FCE_NOERROR)
  Result=Camera.StartDevice();

…
```

Example FireStack API

```
…
// Set framerate

Result=WriteQuad(HIGHOFFSET,m_Props.CmdRegBase+CCR_FRAMERATE,(UINT32)m_Parms.FrameRate<<29
);

 // Set mode
 if(Result)
  Result=WriteQuad(HIGHOFFSET,m_Props.CmdRegBase+CCR_VMODE,(UINT32)m_Parms.VideoMode<<29);

 // Set format
 if(Result)

Result=WriteQuad(HIGHOFFSET,m_Props.CmdRegBase+CCR_VFORMAT,(UINT32)m_Parms.VideoFormat<<29)
;

 // Set trigger
 if(Result)
 {
  Mode=0;
  if(m_Parms.TriggerMode==TM_EXTERN)
   Mode=0x82000000;
  if(m_Parms.TriggerMode==TM_MODE15)
   Mode=0x820F0000;
  WriteQuad(HIGHOFFSET,m_Props.CmdRegBase+CCR_TRGMODE,Mode);
 }

 // Start continous ISO if not oneshot triggermode
 if(Result && m_Parms.TriggerMode!=TM_ONESHOT)
  Result=WriteQuad(HIGHOFFSET,m_Props.CmdRegBase+CCR_ISOENABLE,0x80000000);
…
```

Configuration ROM

The information in the Configuration ROM is needed to identify the node, its capabilities and which drivers are required.

The base address for the `configuration ROM` for all registers is FFFF F0000000h.

Note

If you want to use the `DirectControl` program to read or write to a register, enter the following value in the Address field:

`F0F00000h + Offset`

The ConfigRom is divided into

- Bus info block: providing critical information about the bus-related capabilities
- Root directory: specifying the rest of the content and organization, such as:
  - Node unique ID leaf
  - Unit directory and
  - Unit dependant info

The base address of the camera control register is calculated as follows based on the camera-specific base address:

	Offset	0 to 7	8 to 15	16 to 23	24 to 31	
Bus info block	400h	04	29	0C	C0	
	404h	31	33	39	34	.... ASCII for IEEE1394
	408h	20	00	B2	03	.... Bus capabilities
	40Ch	00	0A	47	01	.... Node_Vendor_Id, Chip_id_hi
	410h	Serial number				.... Chip_id_lo
Root directory	414h	00	04	B7	85	According to IEEE1212, the root directory may have another length. The keys (e.g. 8D) point to the offset factors rather than the offset (e.g. 420h) itself.
	418h	03	00	0A	47	
	41Ch	0C	00	83	C0	
	420h	8D	00	00	02	
	424h	D1	00	00	04	

Table 137: Configuration ROM

The entry with key 8D in the root directory (420h in this case) provides the offset for the Node unique ID leaf.

To compute the effective start address of the node unique ID leaf:

To compute the effective start address of the node unique ID leaf	
currAddr	= node unique ID leaf address
destAddr	= address of directory entry
addrOffset	= value of directory entry
destAddr	= currAddr + (4 * addrOffset)
	= 420h + (4 * 000002h)
	= 428h

Table 138: Computing effective start address

420h + 000002 * 4 = 428h

	Offset	0 to 7	8 to 15	16 to 23	24 to 31	
Node unique ID leaf	428h	00	02	5E	9E	....CRC
	42Ch	00	0A	47	01	....Node_Vendor_Id,Chip_id_hi
	430h	00	00	Serial number		

Table 139: Config ROM

The entry with key D1 in the root directory (424h in this case) provides the offset for the unit directory as follows:

424h + 000004 * 4 = 434h

	Offset	0 to 7	8 to 15	16 to 23	24 to 31
Unit directory	434h	00	03	93	7D
	438h	12	00	A0	2D
	43Ch	13	00	01	02
	440h	D4	00	00	01

Table 140: Config ROM

The entry with key D4 in the unit directory (440h in this case) provides the offset for unit dependent info:

440h + 000001 * 4 = 444h

	Offset	0 to 7	8 to 15	16 to 23	24 to 31	
Unit dependent info	444h	00	0B	A9	6E	....unit_dep_info_length, CRC
	448h	40	3C	00	00	....command_regs_base
	44Ch	81	00	00	02	....vender_name_leaf
	450h	82	00	00	06	....model_name_leaf
	454h	38	00	00	10	....unit_sub_sw_version
	458h	39	00	00	00	....Reserved
	45Ch	3A	00	00	00	....Reserved
	460h	3B	00	00	00	....Reserved
	464h	3C	00	01	00	....vendor_unique_info_0
	468h	3D	00	92	00	....vendor_unique_info_1
	46Ch	3E	00	00	65	....vendor_unique_info_2
	470h	3F	00	00	00	....vendor_unique_info_3

Table 141: Config ROM

And finally, the entry with key 40 (448h in this case) provides the offset for the camera control register:

FFFF F0000000h + 3C0000h * 4 = FFFF F0F00000h

The base address of the camera control register is thus:

FFFF F0F00000h

The offset entered in the table always refers to the base address of F0F00000h.

Implemented registers

The following tables show how standard registers from IIDC V1.31 are implemented in the camera. Base address is F0F00000h. Differences and explanations can be found in the third column.

Camera initialize register

Offset	Name	Description
000h	INITIALIZE	Assert MSB = 1 for Init.

Table 142: Camera initialize register

Video format inquiry register

Offset	Name	Field	Bit	Description
100h	V_FORMAT_INQ	Format_0	[0]	Up to VGA (non compressed)
		Format_1	[1]	SVGA to XGA
		Format_2	[2]	SXGA to UXGA
		Format_3	[3 to 5]	Reserved
		Format_6	[6]	Still Image Format
		Format_7	[7]	Partial Image Format
		---	[8 to 31]	Reserved

Table 143: Format inquiry register

Video mode inquiry register

Offset	Name	Field	Bit	Description	Color mode
180h	V_MODE_INQ (Format_0)	Mode_0	[0]	160 × 120	YUV 4:4:4
		Mode_1	[1]	320 × 240	YUV 4:2:2
		Mode_2	[2]	640 × 480	YUV 4:1:1
		Mode_3	[3]	640 × 480	YUV 4:2:2
		Mode_4	[4]	640 × 480	RGB
		Mode_5	[5]	640 × 480	MONO8
		Mode_6	[6]	640 × 480	MONO16
		Mode_X	[7]	Reserved	
		-	[8 to 31]	Reserved (zero)	
184h	V_MODE_INQ (Format_1)	Mode_0	[0]	800 × 600	YUV 4:2:2
		Mode_1	[1]	800 × 600	RGB
		Mode_2	[2]	800 × 600	MONO8
		Mode_3	[3]	1024 × 768	YUV 4:2:2
		Mode_4	[4]	1024 × 768	RGB
		Mode_5	[5]	1024 × 768	MONO8
		Mode_6	[6]	800 × 600	MONO16
		Mode_7	[7]	1024 × 768	MONO16
		-	[8 to 31]	Reserved (zero)	

Table 144: Video mode inquiry register

Offset	Name	Field	Bit	Description	Color mode
188h	V_MODE_INQ (Format_2)	Mode_0	[0]	1280 × 960	YUV 4:2:2
		Mode_1	[1]	1280 × 960	RGB
		Mode_2	[2]	1280 × 960	MONO8
		Mode_3	[3]	1600 × 1200	YUV 4:2:2
		Mode_4	[4]	1600 × 1200	RGB
		Mode_5	[5]	1600 × 1200	MONO8
		Mode_6	[6]	1280 × 960	MONO16
		Mode_7	[7]	1600 × 1200	MONO16
		-	[8 to 31]	Reserved (zero)	
18Ch … 197h	Reserved for other V_MODE_INQ_x for Format_x.			Always 0	
198h	V_MODE_INQ_6 (Format_6)			Always 0	
19Ch	V_MODE_INQ (Format_7)	Mode_0	[0]	Format_7 Mode_0	
		Mode_1	[1]	Format_7 Mode_1	
		Mode_2	[2]	Format_7 Mode_2	
		Mode_3	[3]	Format_7 Mode_3	
		Mode_4	[4]	Format_7 Mode_4	
		Mode_5	[5]	Format_7 Mode_5	
		Mode_6	[6]	Format_7 Mode_6	
		Mode_7	[7]	Format_7 Mode_7	
		-	[8 to 31]	Reserved (zero)	

Table 144: Video mode inquiry register (continued)

Video frame rate and base address inquiry register

Offset	Name	Field	Bit	Description
200h	V_RATE_INQ (Format_0, Mode_0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		-	[8 to 31]	Reserved (zero)
204h	V_RATE_INQ (Format_0, Mode_1)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		-	[8 to 31]	Reserved (zero)
208h	V_RATE_INQ (Format_0, Mode_2)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register

Offset	Name	Field	Bit	Description
20Ch	V_RATE_INQ (Format_0, Mode_3)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
210h	V_RATE_INQ (Format_0, Mode_4)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
214h	V_RATE_INQ (Format_0, Mode_5)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
218h	V_RATE_INQ	(Format_0, Mode_6) FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
21Ch to 21Fh	Reserved V_RATE_INQ_0_x (for other Mode_x of Format_0)			Always 0
220h	V_RATE_INQ (Format_1, Mode_0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
224h	V_RATE_INQ (Format_1, Mode_1)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
228h	V_RATE_INQ (Format_1, Mode_2)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
22Ch	V_RATE_INQ (Format_1, Mode_3)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
230h	V_RATE_INQ (Format_1, Mode_4)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
234h	V_RATE_INQ (Format_1, Mode_5)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
238h	V_RATE_INQ (Format_1, Mode_6)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	240 fps (V1.31)
		---	[8 to 31]	Reserved (zero)
23Ch	V_RATE_INQ (Format_1, Mode_7)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
240h	V_RATE_INQ (Format_2, Mode_0)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)
244h	V_RATE_INQ (Format_2, Mode_1)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)
248h	V_RATE_INQ (Format_2, Mode_2)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	120 fps (V1.31)
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
24Ch	V_RATE_INQ (Format_2, Mode_3)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)
250h	V_RATE_INQ (Format_2, Mode_4)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	Reserved
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)
254h	V_RATE_INQ (Format_2, Mode_5)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
258h	V_RATE_INQ (Format_2, Mode_6)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved (zero)
25Ch	V_RATE_INQ (Format_2, Mode_7)	FrameRate_0	[0]	1.875 fps
		FrameRate_1	[1]	3.75 fps
		FrameRate_2	[2]	7.5 fps
		FrameRate_3	[3]	15 fps
		FrameRate_4	[4]	30 fps
		FrameRate_5	[5]	60 fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		---	[8 to 31]	Reserved
260h to 2BFh	Reserved V_RATE_INQ_y_x (for other Format_y, Mode_x)			
2C0h	V_REV_INQ_6_0 (Format_6, Mode0)			Always 0
2C4h to 2DFh	Reserved V_REV_INQ_6_x (for other Mode_x of Format_6)			Always 0
2E0h	V-CSR_INQ_7_0		[0 to 31]	CSR_quadlet offset for Format_7 Mode_0
2E4h	V-CSR_INQ_7_1		[0 to 31]	CSR_quadlet offset for Format_7 Mode_1
2E8h	V-CSR_INQ_7_2		[0 to 31]	CSR_quadlet offset for Format_7 Mode_2
2ECh	V-CSR_INQ_7_3		[0 to 31]	CSR_quadlet offset for Format_7 Mode_3
2F0h	V-CSR_INQ_7_4		[0 to 31]	CSR_quadlet offset for Format_7 Mode_4

Table 145: Frame rate inquiry register (continued)

Offset	Name	Field	Bit	Description
2F4h		V-CSR_INQ_7_5	[0 to 31]	CSR_quadlet offset for Format_7 Mode_5
2F8h		V-CSR_INQ_7_6	[0 to 31]	CSR_quadlet offset for Format_7 Mode_6
2FCh		V-CSR_INQ_7_7	[0 to 31]	CSR_quadlet offset for Format_7 Mode_7

Table 145: Frame rate inquiry register (continued)

Basic function inquiry register

Offset	Name	Field	Bit	Description
400h	BASIC_FUNC_INQ	Advanced_Feature_Inq	[0]	Inquiry for advanced features (Vendor unique Features)
		Vmode_Error_Status_Inq	[1]	Inquiry for existence of Vmode_Error_Status register
		Feature_Control_Error_Status_Inq	[2]	Inquiry for existence of Feature_Control_Error_Status
		Opt_Func_CSR_Inq	[3]	Inquiry for Opt_Func_CSR
		---	[4 to 7]	Reserved
		1394b_mode_Capability	[8]	Inquiry for 1394b_mode_Capability
		---	[9 to 15]	Reserved
		Cam_Power_Cntl	[16]	Camera process power ON/ OFF capability
		---	[17 to 18]	Reserved
		One_Shot_Inq	[19]	One Shot transmission capability
		Multi_Shot_Inq	[20]	Multi Shot transmission capability
		---	[21 to 27]	Reserved
		Memory_Channel	[28 to 31]	Maximum memory channel number (N) If 0000, no user memory available

Table 146: Basic function inquiry register

Feature presence inquiry register

Offset	Name	Field	Bit	Description
404h	FEATURE_HI_INQ	Brightness	[0]	Brightness Control
		Auto_Exposure	[1]	Auto_Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White_Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control
		Shutter	[7]	Shutter Control
		Gain	[8]	Gain Control
		Iris	[9]	Iris Control
		Focus	[10]	Focus Control
		Temperature	[11]	Temperature Control
		Trigger	[12]	Trigger Control
		Trigger_Delay	[13]	Trigger_Delay Control
		White_Shading	[14]	White_Shading Control
		Frame_Rate	[15]	Frame_Rate Control
		---	[16 to 31]	Reserved
408h	FEATURE_LO_INQ	Zoom	[0]	Zoom Control
		Pan	[1]	Pan Control
		Tilt	[2]	Tilt Control
		Optical_Filter	[3]	Optical_Filter Control
		---	[4 to 15]	Reserved
		Capture_Size	[16]	Capture_Size for Format_6
		Capture_Quality	[17]	Capture_Quality for Format_6
		---	[16 to 31]	Reserved
40Ch	OPT_FUNCTION_INQ	---	[0]	Reserved
		PIO	[1]	Parallel Input/Output control
		SIO	[2]	Serial Input/Output control
		Strobe_out	[4 to 31]	Strobe signal output
410h to 47Fh	Reserved			Address error on access

Table 147: Feature presence inquiry register

Offset	Name	Field	Bit	Description
480h	Advanced_Feature_Inq	Advanced_Feature_Quadlet_Offset	[0 to 31]	Quadlet offset of the advanced feature CSR's from the base address of initial register space (vendor unique) This register is the offset for the Access_Control_Register and thus the base address for Advanced Features. Access_Control_Register does not prevent access to advanced features. In some programs it should still always be activated first. `Advanced Feature Set Unique Value` is 7ACh and `CompanyID` is A47h.
484h	PIO_Control_CSR_Inq	PIO_Control_Quadlet_Offset	[0 to 31]	Quadlet offset of the PIO_Control CSR's from the base address of initial register space (Vendor unique)
488h	SIO_Control_CSR_Inq	SIO_Control_Quadlet_Offset	[0 to 31]	Quadlet offset of the SIO_Control CSR's from the base address of initial register space (Vendor unique)
48Ch	Strobe_Output_CSR_Inq	Strobe_Output_Quadlet_Offset	[0 to 31]	Quadlet offset of the Strobe_Output signal CSR's from the base address of initial register space (vendor unique)

Table 147: Feature presence inquiry register (continued)

Feature elements inquiry register

Register	Name	Field	Bit	Description
0xF0F00500	BRIGHTNESS_INQUIRY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Abs_Control_Inq	[1]	Capability of control with absolute value
		-	[2]	Reserved
		One_Push_Inq	[3]	One Push auto mode (Controlled automatically by the camera once)
		Readout_Inq	[4]	Capability of reading out the value of this feature
		ON_OFF	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Auto Mode (Controlled automatically by the camera)
		Manual_Inq	[7]	Manual Mode (Controlled by user)
		Min_Value	[8 to 19]	Minimum value for this feature
		Max_Value	[20 to 31]	Maximum value for this feature
504h	AUTO_EXPOSURE_INQ	Same definition as Brightness_inq.		
508h	SHARPNESS_INQ	Same definition as Brightness_inq.		
50Ch	WHITE_BAL_INQ	Same definition as Brightness_inq.		
510h	HUE_INQ	Same definition as Brightness_inq.		
514h	SATURATION_INQ	Same definition as Brightness_inq.		
518h	GAMMA_INQ	Same definition as Brightness_inq.		
51Ch	SHUTTER_INQ	Same definition as Brightness_inq.		
520h	GAIN_INQ	Same definition as Brightness_inq.		
524h	IRIS_INQ	Always 0		
528h	FOCUS_INQ	Always 0		
52Ch	TEMPERATURE_INQ	Same definition as Brightness_inq.		

Table 148: Feature elements inquiry register

Register	Name	Field	Bit	Description
530h	TRIGGER_INQ	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Abs_Control_Inq	[1]	Capability of control with absolute value
		---	[2 to 3]	Reserved
		Readout_Inq	[4]	Capability of reading out the value of this feature
		ON_OFF	[5]	Capability of switching this feature ON and OFF
		Polarity_Inq	[6]	Capability of changing the polarity of the trigger input
		---	[7 to 15]	Reserved
		Trigger_Mode0_Inq	[16]	Presence of Trigger_Mode 0
		Trigger_Mode1_Inq	[17]	Presence of Trigger_Mode 1
		Trigger_Mode2_Inq	[18]	Presence of Trigger_Mode 2
		Trigger_Mode3_Inq	[19]	Presence of Trigger_Mode 3
		---	[20 to 31]	Reserved
534h	TRIGGER_DELAY_INQUIRY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Abs_Control_Inq	[1]	Capability of control with absolute value
		---	[2]	Reserved
		One_Push_Inq	[3]	One Push auto mode Controlled automatically by the camera once)
		Readout_Inq	[4]	Capability of reading out the value of this feature
		ON_OFF	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Auto Mode (Controlled automatically by the camera)
		Manual_Inq	[7]	Manual Mode (Controlled by user)
		Min_Value	[8 to 19]	Minimum value for this feature
		Max_Value	[20 to 31]	Maximum value for this feature

Table 148: Feature elements inquiry register (continued)

Register	Name	Field	Bit	Description
538 .. 57Ch	Reserved for other FEATURE_HI_INQ			
580h	ZOOM_INQ	Always 0		
584h	PAN_INQ	Always 0		
588h	TILT_INQ	Always 0		
58Ch	OPTICAL_FILTER_INQ	Always 0		
590 to 5BCh	Reserved for other FEATURE_LO_INQ	Always 0		
5C0h	CAPTURE_SIZE_INQ	Always 0		
5C4h	CAPTURE_QUALITY_INQ	Always 0		
5C8h to 5FCh	Reserved for other FEATURE_LO_INQ	Always 0		
600h	CUR-V-Frm_RATE/ Revision	Bits [0 to 2] for the frame rate		
604h	CUR-V-MODE	Bits [0 to 2] for the current video mode		
608h	CUR-V-FORMAT	Bits [0 to 2] for the current video format		
60Ch	ISO-Channel	Bits [0 to 3] for channel, [6 to 7] for ISO speed		
610h	Camera_Power	Always 0		
614h	ISO_EN/ Continuous_Shot	Bit 0: 1 for start continuous shot; 0 for stop continuos shot		
618h	Memory_Save	Always 0		
61Ch	One_Shot, Multi_Shot, Count Number	See One-shot on page 185 See Multi-shot on page 187		
620h	Mem_Save_Ch	Always 0		
624	Cur_Mem_Ch	Always 0		
628h	Vmode_Error_Status	Error in combination of Format/Mode/ISO Speed: Bit(0): No error; Bit(0)=1: error		

Table 148: Feature elements inquiry register (continued)

Absolute value CSR offset address inquiry register

Offset	Name	Notes
700h	ABS_CSR_HI_INQ_0	Always 0
704h	ABS_CSR_HI_INQ_1	Always 0
708h	ABS_CSR_HI_INQ_2	Always 0
70Ch	ABS_CSR_HI_INQ_3	Always 0
710h	ABS_CSR_HI_INQ_4	Always 0
714h	ABS_CSR_HI_INQ_5	Always 0
718h	ABS_CSR_HI_INQ_6	Always 0
71Ch	ABS_CSR_HI_INQ_7	Always 0
720h	ABS_CSR_HI_INQ_8	Always 0
724h	ABS_CSR_HI_INQ_9	Always 0
728h	ABS_CSR_HI_INQ_10	Always 0
72Ch	ABS_CSR_HI_INQ_11	Always 0
730h	ABS_CSR_HI_INQ_12	Always 0
734 to 77Fh	Reserved	Always 0
780h	ABS_CSR_LO_INQ_0	Always 0
784h	ABS_CSR_LO_INQ_1	Always 0
788h	ABS_CSR_LO_INQ_2	Always 0
78Ch	ABS_CSR_LO_INQ_3	Always 0
790h .. 7BFh	Reserved	Always 0
7C0h	ABS_CSR_LO_INQ_16	Always 0
7C4h	ABS_CSR_LO_INQ_17	Always 0
7C8h .. 7FFh	Reserved	Always 0

Table 149: Absolute value inquiry register

Status and control register for feature

The `OnePush` feature, WHITE_BALANCE, is currently implemented. If this flag is set, the feature becomes immediately active, even if no images are being input (see One-push white balance on page 109).

Offset	Name	Field	Bit	Description
800h	BRIGHTNESS	Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
		Abs_Control	[1]	Absolute value control 0: Control with value in the `Value` field 1: Control with value in the Absolute value CSR If this bit = 1, value in the `Value` field is ignored.
		---	[2 to 4]	Reserved
		One_Push	[5]	Write 1: begin to work (Self cleared after operation) Read: Value=1 in operation Value=0 not in operation If A_M_Mode =1, this bit is ignored.
		ON_OFF	[6]	Write: ON or OFF this feature Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		A_M_Mode	[7]	Write: set the mode Read: read a current mode 0: Manual 1: Auto
		---	[8 to 19]	Reserved
		Value	[20 to 31]	Value. Write the value in Auto mode, this field is ignored. If `ReadOut` capability is not available, read value has no meaning.
804h	AUTO-EXPOSURE			See above Note: `Target gray level` parameter in SmartView corresponds to Auto_exposure register 0xF0F00804 (IIDC).
808h	SHARPNESS			See above

Table 150: Feature control register

Offset	Name	Field	Bit	Description
80Ch	WHITE-BALANCE	Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available Always 0 for Mono
		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		--	[2 to 4]	Reserved
		One_Push	[5]	Write 1: begin to work (Self cleared after operation) Read: Value=1 in operation Value=0 not in operation If A_M_Mode =1, this bit is ignored.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF 1: ON If this bit =0, other fields will be read only.
		A_M_Mode	[7]	Write: set the mode Read: read a current mode 0: Manual 1: Auto
		U_Value / B_Value	[8 to 19]	U value / B value Write the value in AUTO mode, this field is ignored. If `ReadOut` capability is not available, read value has no meaning.
		V_Value / R_Value	[20 to 31]	V value / R value Write the value in AUTO mode, this field is ignored. If `ReadOut` capability is not available, read value has no meaning.

Table 150: Feature control register (continued)

Offset	Name	Field	Bit	Description
810h	HUE			See above Always 0 for Mono
814h	SATURATION			See above Always 0 for Mono
818h	GAMMA			See above
81Ch	SHUTTER			See Advanced Feature time base See Table 44: CSR: Shutter on page 113
820h	GAIN			See above
824h	IRIS			Always 0
828h	FOCUS			Always 0
82Ch	TEMPERATURE			Always 0
830h	TRIGGER-MODE			Can be effected via advanced feature IO_INP_CTRLx.
834h to 87C	Reserved for other FEATURE_HI			Always 0
880h	Zoom			Always 0
884h	PAN			Always 0
888h	TILT			Always 0
88Ch	OPTICAL_FILTER			Always 0
890 to 8BCh	Reserved for other FEATURE_LO			Always 0
8C0h	CAPTURE-SIZE			Always 0
8C4h	CAPTURE-QUALITY			Always 0
8C8h to 8FCh	Reserved for other FEATURE_LO			Always 0

Table 150: Feature control register (continued)

Feature control error status register

Offset	Name	Notes
640h	Feature_Control_Error_Status_HI	Always 0
644h	Feature_Control_Error_Status_LO	Always 0

Table 151: Feature control error register

Video mode control and status registers for Format_7

Quadlet offset Format_7 Mode_0

The quadlet offset to the base address for `Format_7 Mode_0`, which can be read out at F0F002E0h (according to Table 145: Frame rate inquiry register on page 267) gives 003C2000h.

4 × 3C2000h = F08000h so that the base address for the latter (Table 152: Format_7 control and status register on page 285) equals
F0000000h + F08000h = F0F08000h.

Quadlet offset Format_7 Mode_1

The quadlet offset to the base address for `Format_7 Mode_1`, which can be read out at F0F002E4h (according to Table 145: Frame rate inquiry register on page 267) gives 003C2400h.

4 × 003C2400h = F09000h so that the base address for the latter (Table 152: Format_7 control and status register on page 285) equals
F0000000h + F09000h = F0F09000h.

Format_7 control and status register (CSR)

Offset	Name	Notes
000h	MAX_IMAGE_SIZE_INQ	According to IIDC V1.31
004h	UNIT_SIZE_INQ	According to IIDC V1.31
008h	IMAGE_POSITION	According to IIDC V1.31
00Ch	IMAGE_SIZE	According to IIDC V1.31
010h	COLOR_CODING_ID	See note
014h	COLOR_CODING_INQ	According to IIDC V1.31

Table 152: Format_7 control and status register

Offset	Name	Notes

024h
.
.
033h
	COLOR_CODING_INQ	Vendor Unique Color_Coding
		0-127 (ID=128-255)
		`ID=132ECCID_MONO12`
		`ID=136ECCID_RAW12`
		ID=133Reserved
		ID=134Reserved
		ID=135Reserved
		See **Packed 12-Bit Mode** on page 158.

034h	PIXEL_NUMER_INQ	According to IIDC V1.31
038h	TOTAL_BYTES_HI_INQ	According to IIDC V1.31
03Ch	TOTAL_BYTES_LO_INQ	According to IIDC V1.31
040h	PACKET_PARA_INQ	See note
044h	BYTE_PER_PACKET	According to IIDC V1.31

Table 152: Format_7 control and status register (continued)

Note

- For all modes in Format_7, `ErrorFlag_1` and `ErrorFlag_2` are refreshed on each access to the Format_7 Register.
- Contrary to IIDC DCAM V1.31, registers relevant to Format_7 are refreshed on each access. The `Setting_1` bit is automatically cleared after each access.
- When `ErrorFlag_1` or `ErrorFlag_2` are set and Format_7 is configured, no image capture is started.
- Contrary to IIDC V1.31, COLOR_CODING_ID is set to a default value after an INITIALIZE or `reset`.
- Contrary to IIDC V1.31, the `UnitBytePerPacket` field is already filled in with a fixed value in the PACKET_PARA_INQ register.

Advanced features

The camera has a variety of extended features going beyond the possibilities described in IIDC V1.31. The following chapter summarizes all available advanced features in ascending register order.

Note

This chapter is a `reference guide for advanced registers` and does not explain the advanced features itself.

For detailed description of the theoretical background see

- Description of the data path on page 102
- Links given in the table below

The following table gives an overview of all available registers:

Register	Register name	Remarks
0xF1000010	VERSION_INFO1	See Table 154: Advanced register: Extended version information on page 291
0xF1000018	VERSION_INFO3	
0xF1000040	ADV_INQ_1	See Table 156: Advanced register: Advanced feature inquiry on page 293 In ADV_INQ_3 there are two new fields: • Paramupd_Timing [2] • F7MODE_MAPPING [3]
0xF1000044	ADV_INQ_2	
0xF1000048	ADV_INQ_3	
0xF100004C	ADV_INQ_4	
0xF1000100	CAMERA_STATUS	See Table 157: Advanced register: Camera status on page 295
0xF1000200	MAX_RESOLUTION	See Table 158: Advanced register: Maximum resolution inquiry on page 296
0xF1000208	TIMEBASE	See Table 159: Advanced register: Time base on page 296
0xF100020C	EXTD_SHUTTER	See Table 161: Advanced register: Extended shutter on page 297
0xF1000210	TEST_IMAGE	See Table 162: Advanced register: Test image on page 299
0xF1000220	SEQUENCE_CTRL	Table 81: Advanced register: **Sequence mode** on page 191
0xF1000224	SEQUENCE_PARAM	
0xF1000228	SEQUENCE_STEP	
0xF1000240	LUT_CTRL	See Table 163: Advanced register: LUT on page 300
0xF1000244	LUT_MEM_CTRL	
0xF1000248	LUT_INFO	

Table 153: Advanced registers summary

Register	Register name	Remarks
0xF1000250	SHDG_CTRL	See Table 164: Advanced register: Shading on page 302
0xF1000254	SHDG_MEM_CTRL	
0xF1000258	SHDG_INFO	
0xF1000260	DEFERRED_TRANS	See Table 166: Advanced register: Deferred image transport on page 305
0xF1000270	FRAMEINFO	See Table 167: Advanced register: Frame information on page 306
0xF1000274	FRAMECOUNTER	
0xF1000300	IO_INP_CTRL1	See Table 25: Advanced register: **Input control** on page 87
0xF1000304	IO_INP_CTRL2	
0xF1000308	IO_INP_CTRL3	
0xF100030C	IO_INP_CTRL4	
0xF1000320	IO_OUTP_CTRL1	See Table 31: Advanced register: **Output control** on page 91
0xF1000324	IO_OUTP_CTRL2	
0xF1000328	IO_OUTP_CTRL3	
0xF100032C	IO_OUTP_CTRL4	
0xF1000340	IO_INTENA_DELAY	See Table 168: Advanced register: Delayed Integration Enable on page 307
0xF1000360	AUTOSHUTTER_CTRL	See Table 169: Advanced register: Auto shutter control on page 307
0xF1000364	AUTOSHUTTER_LO	
0xF1000368	AUTOSHUTTER_HI	
0xF1000370	AUTOGAIN_CTRL	See Table 170: Advanced register: Auto gain control on page 309
0xF1000390	AUTOFNC_AOI	See Table 171: Advanced register: Autofunction AOI on page 310
0xF1000394	AF_AREA_POSITION	
0xF1000398	AF_AREA_SIZE	
0xF10003A0	COLOR_CORR	Pike color cameras only See Table 172: Advanced register: Color correction on page 311

Table 153: Advanced registers summary (continued)

Register	Register name	Remarks
0xF10003A4	COLOR_CORR_COEFFIC11 = Crr	Pike color camera only See Table 172: Advanced register: Color correction on page 311
0xF10003A8	COLOR_CORR_COEFFIC12 = Cgr	
0xF10003AC	COLOR_CORR_COEFFIC13 = Cbr	
0xF10003B0	COLOR_CORR_COEFFIC21 = Crg	
0xF10003B4	COLOR_CORR_COEFFIC22 = Cgg	
0xF10003B8	COLOR_CORR_COEFFIC23 = Cbg	
0xF10003BC	COLOR_CORR_COEFFIC31 = Crb	
0xF10003C0	COLOR_CORR_COEFFIC32 = Cgb	
0xF10003C4	COLOR_CORR_COEFFIC33 = Cbb	
0xF1000400	TRIGGER_DELAY	See Table 173: Advanced register: Trigger delay on page 312
0xF1000410	MIRROR_IMAGE	See Table 174: Advanced register: Mirror image on page 312
0xF1000420	AFE_CHN_COMP	See Table 175: Advanced register: Channel balance on page 313
0xF1000424		
0xF1000428		
0xF1000430	DUAL TAP OFFSET ADJUSTMENT	See Table 176: Advanced register: Dual-tap offset adjustment on page 313
0xF1000434		
0xF1000440	LOW_SMEAR	See Smear reduction (not Pike F-1100, F-1600) on page 328
0xF1000460	DEFECT_PIXEL_CORRECTION_C-TRL	See Table 194: Advanced register: Defect pixel correction on page 329
0xF1000510	SOFT_RESET	See Table 177: Advanced register: Soft reset on page 314
0xF1000520	HIGH_SNR	See Table 178: Advanced register: High Signal Noise Ratio (HSNR) on page 315
0xF1000550	USER PROFILES	See Table 195: Advanced register: User profiles on page 331
0xF1000560	F7MODE_MAPPING	See Table 186: Advanced register: Format_7 mode mapping on page 322
0xF1000570	PARAMUPD_TIMING	See Quick parameter change timing modes on page 317
0xF10005B0	LOW_NOISE_BINNING	See Low-noise binning mode (only 2 × H-binning) on page 319
0xF1000620	TRIGGER_COUNTER	See Table 191: Advanced register: Trigger counter on page 327
0xF1000630	SIS	

Table 153: Advanced registers summary (continued)

Register	Register name	Remarks
0xF1000640	SWFEATURE_CTRL	See Table 183: Advanced register: Software feature control (disable LEDs/switch single-tap and dual-tap) on page 320
0xF1000800 0xF1000804	IO_OUTP_PWM1	See Table 33: PWM configuration registers on page 94
0xF1000808 0xF100080C	IO_OUTP_PWM2	
0xF1000810 0xF1000814	IO_OUTP_PWM3	
0xF1000818 0xF100081C	IO_OUTP_PWM4	
0xF1000840	IO_INP_DEBOUNCE_1	
0xF1000850	IO_INP_DEBOUNCE_2	
0xF1000860	IO_INP_DEBOUNCE_3	
0xF1000870	IO_INP_DEBOUNCE_4	
0xF1000A00	FRAMETIME_CTRL	See Frame time control on page 334
0xF1000A04		
0xF1000A08		
0xF1000FFC	GPDATA_INFO	See Table 199: Advanced register: GPData buffer on page 335
0xF1001000 … 0xF100nnnn	GPDATA_BUFFER	
0xF1100000	PARRAMLIST_INFO	See Parameter-List Update on page 321
0xF1101000	PARAMLIST_BUFFER	
0xF1002000	AFEREFERENCES	See User adjustable gain references on page 336

Table 153: Advanced registers summary (continued)

Note

Advanced features should always be activated before accessing them.

Note

- Currently all registers can be written without being activated. This makes it easier to operate the camera using `Directcontrol`.
- Allied Vision reserves the right to require activation in future versions of the software.

Extended version information register

The presence of each of the following features can be queried by the `0` bit of the corresponding register.

Register	Name	Field	Bit	Description
0xF1000010	VERSION_INFO1	µC type ID	[0 to 15]	Always 0
		µC version	[16 to 31]	Bcd-coded version number
0xF1000014	VERSION_INFO1_EX	µC version	[0 to 31]	Bcd-coded version number
0xF1000018	VERSION_INFO3	Camera type ID	[0 to 15]	See Table 155: Camera type ID list on page 292.
		FPGA version	[16 to 31]	Bcd-coded version number
0xF100001C	VERSION_INFO3_EX	FPGA version	[0 to 31]	Bcd-coded version number
0xF1000020		---	[0 to 31]	Reserved
0xF1000024		---	[0 to 31]	Reserved
0xF1000028		---	[0 to 31]	Reserved
0xF100002C		---	[0 to 31]	Reserved
0xF1000030		OrderIDHigh	[0 to 31]	8 Byte ASCII Order ID
0xF1000034		OrderIDLow	[0 to 31]	

Table 154: Advanced register: Extended version information

The µC version and FPGA firmware version numbers are bcd-coded, which means that e.g. firmware version 0.85 is read as 0x0085 and version 1.10 is read as 0x0110.

The newly added `VERSION_INFOx_EX` registers contain extended bcd-coded version information formatted as *special.major.minor.patch*.

So reading the value `0x00223344` is decoded as:

- special: 0(decimal)
- major: 22(decimal)
- minor: 33(decimal)
- patch: 44(decimal)

This is decoded to the human readable version `22.33.44` (leading zeros are omitted).

Note

If a camera returns the register set to all zero, that particular camera does not support the extended version information.

The FPGA type ID (= camera type ID) identifies the camera type with the help of the following list:

ID	Camera type
101	Pike F-032B
102	Pike F-032C
103	Pike F-100B
104	Pike F-100C
105	Pike F-145B
106	Pike F-145C
107	Pike F-210B
108	---
109	---
110	---
111	Pike F-421B
112	Pike F-421C
113	---
114	---
115	Pike F-145B-15fps
116	Pike F-145C-15fps
117	Pike F-505B
118	Pike F-505C
119	---
120	---
121	---
122	---
123	Pike F-1100B
124	Pike F-1100C
125	Pike F-1600B
126	Pike F-1600C

Table 155: Camera type ID list

Advanced feature inquiry

This register indicates with a named bit if a feature is present or not. If a feature is marked as not present the associated register space might not be available and read/write errors may occur.

Note

Ignore unnamed bits in the following table: these bits might be set or not.

Register	Name	Field	Bit	Description
0xF1000040	ADV_INQ_1	MaxResolution	[0]	
		TimeBase	[1]	
		ExtdShutter	[2]	
		TestImage	[3]	
		FrameInfo	[4]	
		Sequences	[5]	
		VersionInfo	[6]	
		---	[7]	Reserved
		Look-up tables	[8]	
		Shading	[9]	
		DeferredTrans	[10]	
		HDR mode	[11]	
		---	[12]	Reserved
		---	[13]	Reserved
		TriggerDelay	[14]	
		Mirror image	[15]	
		Soft Reset	[16]	
		High SNR	[17]	
		Color Correction	[18]	
		---	[19 to 20]	Reserved
		User Sets	[21]	
		---	[22 to 29]	Reserved
		Paramlist_Info	[30]	
		GP_Buffer	[31]	

Table 156: Advanced register: Advanced feature inquiry

Register	Name	Field	Bit	Description
0xF1000044	ADV_INQ_2	Input_1	[0]	
		Input_2	[1]	
		---	[2 to 7]	Reserved
		Output_1	[8]	
		Output_2	[9]	
		Output_3	[10]	
		Output_4	[11]	
		---	[12 to 15]	Reserved
		IntEnaDelay	[16]	
		---	[17 to 23]	Reserved
		Output 1 PWM	[24]	
		Output 2 PWM	[25]	
		Output 3 PWM	[26]	
		Output 4 PWM	[27]	
		---	[28 to 31]	Reserved
0xF1000048	ADV_INQ_3	Camera Status	[0]	
		Max IsoSize	[1]	
		Paramupd_Timing	[2]	
		F7 mode mapping	[3]	
		Auto Shutter	[4]	
		Auto Gain	[5]	
		Auto FNC AOI	[6]	
		---	[7 to 31]	Reserved
0xF100004C	ADV_INQ_4	HDR Pike	[0]	
		Channel Compensation	[1]	
		Smear reduction	[2]	Not Pike F-1100, F-1600
		---	[18 to 31]	Reserved

Table 156: Advanced register: Advanced feature inquiry (continued)

Camera status

This register allows to determine the current status of the camera. The most important flag is the `Idle` flag.

If the `Idle` flag is set the camera does not capture and does not send any images (but images might be present in the image FIFO).

The `ExSyncArmed` flag indicates that the camera is set up for external triggering. Even if the camera is waiting for an external trigger event the `Idle` flag might get set.

Other bits in this register might be set or toggled: just ignore these bits.

Note

- Excessive polling of this register may slow down the operation of the camera. Therefore the time between two polls of the status register should not be less than 5 milliseconds. If the time between two read accesses is lower than 5 milliseconds the response will be delayed.
- Depending on shutter and isochronous settings the status flags might be set for a very short time and thus will not be recognized by your application.

Register	Name	Field	Bit	Description
0xF1000100	CAMERA_STATUS	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 23]	Reserved
		ID	[24 to 31]	Implementation ID = 0x01
0xF1000104		---	[0 to 14]	Reserved
		ExSyncArmed	[15]	External trigger enabled
		---	[16 to 27]	Reserved
		ISO	[28]	Isochronous transmission
		---	[29 to 30]	Reserved
		Idle	[31]	Camera idle

Table 157: Advanced register: Camera status

Maximum resolution

This register indicates the highest resolution for the sensor and is read-only.

Note

This register normally outputs the MAX_IMAGE_SIZE_INQ Format_7 Mode_0 value.

This is the value given in the specifications tables under `Picture size (maximum)` in Specifications on page 45ff.

Register	Name	Field	Bit	Description
0xF1000200	MAX_RESOLUTION	MaxHeight	[0 to 15]	Sensor height (read only)
		MaxWidth	[16 to 31]	Sensor width (read only)

Table 158: Advanced register: Maximum resolution inquiry

Time base

Corresponding to IIDC, exposure time is set via a 12-bit value in the corresponding register (SHUTTER_INQ [51Ch] and SHUTTER [81Ch]).

This means that you can enter a value in the range of 1 to 4095.

Pike cameras use a time base which is multiplied by the shutter register value. This multiplier is configured as the time base via the TIMEBASE register.

Register	Name	Field	Bit	Description
0xF1000208	TIMEBASE	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 7]	Reserved
		ExpOffset	[8 to 19]	Exposure offset in µs
		---	[20 to 27]	Reserved
		Timebase_ID	[28 to 31]	See Table 160: Time base ID on page 297.

Table 159: Advanced register: Time base

The time base IDs 0 to 9 are in bit [28] to [31]. See Table 160: Time base ID on page 297.

Default time base is 20 µs: This means that the integration time can be changed in 20 µs increments with the shutter control.

Note

Time base can only be changed when the camera is in idle state and becomes active only after setting the shutter value.

The `ExpOffset` field specifies the camera specific exposure time offset in microseconds (µs). This time (which should be equivalent to Table 73: Camera-specific exposure time offset on page 183) has to be added to the exposure time (set by any shutter register) to compute the real exposure time.

The `ExpOffset` field might be zero for some cameras: this has to be assumed as an unknown exposure time offset (according to former software versions).

ID	Time base in µs	
0	1	
1	2	
2	5	
3	10	
4	20	Default value
5	50	
6	100	
7	200	
8	500	
9	1000	

Table 160: Time base ID

Note

The ABSOLUTE VALUE CSR register, introduced in IIDC V1.3, is not implemented.

Extended shutter

The exposure time for long-term integration of up to 67 seconds can be entered with µs precision via the EXTENDED_SHUTTER register.

Register	Name	Field	Bit	Description
0xF100020C	EXTD_SHUTTER	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ExpTime	[6 to 31]	Exposure time in µs

Table 161: Advanced register: Extended shutter

The minimum allowed exposure time depends on the camera model. To determine this value write `1` to the `ExpTime` field and read back the minimum allowed exposure time.

The longest exposure time, 3FFFFFFh, corresponds to 67.11 seconds.

Note

- Exposure times entered via the 81Ch register are mirrored in the extended register, but not vice versa.
- Changes in this register have immediate effect, even when camera is transmitting.
- Extended shutter becomes inactive after writing to a format / mode / frame rate register.
- Extended shutter setting will thus be overwritten by the normal time base/shutter setting after Stop/Start of FireView or FireDemo.

Test images

Bit [8] to [14] indicate which test images are saved. Setting bit [28] to [31] activates or deactivates existing test images.

By activating any test image the following auto features are automatically disabled:

- auto gain
- auto shutter
- auto white balance

Register	Name	Field	Bit	Description
0xF1000210	TEST_IMAGE	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 7]	Reserved
		Image_Inq_1	[8]	Presence of test image 1 0: N/A 1: Available
		Image_Inq_2	[9]	Presence of test image 2 0: N/A 1: Available
		Image_Inq_3	[10]	Presence of test image 3 0: N/A 1: Available
		Image_Inq_4	[11]	Presence of test image 4 0: N/A 1: Available
		Image_Inq_5	[12]	Presence of test image 5 0: N/A 1: Available
		Image_Inq_6	[13]	Presence of test image 6 0: N/A 1: Available
		Image_Inq_7	[14]	Presence of test image 7 0: N/A 1: Available
		---	[15 to 27]	Reserved
		TestImage_ID	[28 to 31]	0: No test image active 1: Image 1 active 2: Image 2 active ...

Table 162: Advanced register: Test image

Look-up tables (LUT)

Load the look-up tables to be used into the camera and choose the look-up table number via the `LutNo` field. Now you can activate the chosen LUT via the LUT_CTRL register.

The LUT_INFO register indicates how many LUTs the camera can store and shows the maximum size of the individual LUTs.

The possible values for `LutNo` are 0..n-1, whereas n can be determined by reading the field `NumOfLuts` of the LUT_INFO register.

Register	Name	Field	Bit	Description
0xF1000240	LUT_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Enable/disable this feature
		---	[7 to 25]	Reserved
		LutNo	[26 to 31]	Use look-up table with `LutNo` number
0xF1000244	LUT_MEM_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 4]	Reserved
		EnableMemWR	[5]	Enable write access
		---	[6 to 7]	Reserved
		AccessLutNo	[8 to 15]	Reserved
		AddrOffset	[16 to 31]	byte
0xF1000248	LUT_INFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 2]	Reserved
		BitsPerValue	[3 to 7]	Bits used per table item
		NumOfLuts	[8 to 15]	Maximum number of look-up tables
		MaxLutSize	[16 to 31]	Maximum look-up table size (bytes)

Table 163: Advanced register: LUT

Note

The `BitsPerValue` field indicates how many bits are read from the LUT for any gray-value read from the sensor. To determine the number of bytes occupied for each gray-value round-up the `BitsPerValue` field to the next byte boundary.

Examples:

- BitsPerValue = 8 → 1 byte per gray-value
- BitsPerValue = 14 → 2 byte per gray-value

Divide `MaxLutSize` by the number of bytes per gray-value in order to get the number of bits read from the sensor.

Note

Pike cameras have the gamma feature implemented via a built-in look-up table. Therefore you can not use gamma and your own look-up table at the same time. Nevertheless you may combine a gamma look-up table into your own look-up table.

Note

When using the LUT feature and the gamma feature pay attention to the following:

- gamma ON → look-up table is switched ON also
- gamma OFF → look-up table is switched OFF also
- look-up table OFF → gamma is switched OFF also
- look-up table ON → gamma is switched OFF

Loading a look-up table into the camera

Loading a look-up table into the camera is done through the GPDATA_BUFFER. Because the size of the GPDATA_BUFFER is smaller than a complete look-up table the data must be written in multiple steps.

To load a lookup table into the camera:

1. Query the limits and ranges by reading LUT_INFO and GPDATA_INFO.
2. Set `EnableMemWR` to true (1).
3. Set `AccessLutNo` to the desired number.
4. Set `AddrOffset` to 0.
5. Write n lookup table data bytes to GPDATA_BUFFER (n might be lower than the size of the GPDATA_BUFFER; AddrOffset is automatically adjusted inside the camera).
6. Repeat step 5 until all data is written into the camera.
7. Set `EnableMemWR` to false (0).

Shading correction

Owing to technical circumstances, the interaction of recorded objects with one another, optical effects and lighting non-homogeneities may occur in the images.

Because these effects are normally not desired, they should be eliminated as far as possible in subsequent image editing. The camera has automatic shading correction to do this.

Provided that a shading image is present in the camera, the `on/off` bit can be used to enable shading correction.

The `on/off` and `ShowImage` bits must be set for saved shading images to be displayed.

Note

- Always make sure that the shading image is saved at the highest resolution of the camera. If a lower resolution is chosen and ShowImage is set to `true`, the image will not be displayed correctly.
- The shading image is computed using the current video settings. On fixed video modes the selected frame rate also affects the computation time.
- The build process will not work, if a MONO16/RGB16 format is active.

Register	Name	Field	Bit	Description
0xF1000250	SHDG_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		BuildError	[1]	Could not built shading image
		---	[2 to 3]	Reserved
		ShowImage	[4]	Show shading data as image
		BuildImage	[5]	Build a new shading image
		ON_OFF	[6]	Shading on/off
		Busy	[7]	Build in progress
		MemChannelSave	[8]	Save shading data in flash memory
		MemChannelLoad	[9]	Load shading data from flash memory
		MemChannelClear	[10]	Erase flash memory
		---	[11 to 15]	Reserved
		MemChannelError	[16 to 19]	Indicates memory channel error. See Table 165: Memory channel error description on page 304.
		MemoryChannel	[20 to 23]	Set memory channel number for save and load operations
		GrabCount	[24 to 31]	Number of images

Table 164: Advanced register: Shading

Register	Name	Field	Bit	Description
0xF1000254	SHDG_MEM_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 4]	Reserved
		EnableMemWR	[5]	Enable write access
		EnableMemRD	[6]	Enable read access
		---	[7]	Reserved
		AddrOffset	[8 to 31]	In bytes
0xF1000258	SHDG_INFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 3]	Reserved
		MaxMemChannel	[4 to 7]	Maximum number of available memory channels to store shading images
		MaxImageSize	[8 to 31]	Maximum shading image size (in bytes)

Table 164: Advanced register: Shading (continued)

Reading or writing shading image from/into the camera

Accessing the shading image inside the camera is done through the GPDATA_BUFFER. Because the size of the GPDATA_BUFFER is smaller than a whole shading image the data must be written in multiple steps.

To read or write a shading image:

1. Query the limits and ranges by reading SHDG_INFO and GPDATA_INFO.
2. Set `EnableMemWR` or `EnableMemRD` to true (1).
3. Set `AddrOffset` to 0.
4. Write n shading data bytes to GPDATA_BUFFER (n might be lower than the size of the GPDATA_BUFFER; AddrOffset is automatically adjusted inside the camera).
5. Repeat step 4 until all data is written into the camera.
6. Set `EnableMemWR` and `EnableMemRD` to false.

Automatic generation of a shading image

Shading image data may also be generated by the camera. To use this feature make sure all settings affecting an image are set properly. The camera uses the current active resolution to generate the shading image.

To generate a shading image:

1. Set `GrabCount` to the number of the images to be averaged before the correction factors are calculated.
2. Set `BuildImage` to true.

3. Poll the SHDG_CTRL register until the `Busy` and `BuildImage` flags are reset automatically.

The maximum value of GrabCount depends on the camera type and the number of available image buffers. GrabCount is automatically adjusted to a power of two.

Do not poll the SHDG_CTRL register too often, while automatic generation is in progress. Each poll delays the process of generating the shading image. An optimal poll interval time is 500 ms.

Non-volatile memory operations

Pike cameras support storing shading image data into non-volatile memory. Once a shading image is stored it is automatically reloaded on each camera reset.

`MaxMemChannel` indicates the number of so-called memory channels/slots available for storing shading images.

To store a shading image into non-volatile memory:

1. Set `MemoryChannel` to the desired memory channel and `MemoryChannelSave` to true (1).
2. Read `MemoryChannelError` to check for errors.

To reload a shading image from non-volatile memory:

1. Set `MemoryChannel` to the desired memory channel and `MemChannelLoad` to true (1).
2. Read `MemChannelError` to check for errors.

To clear already stored shading image data in non-volatile memory (shading image data won't be loaded on camera resets):

1. Set `MemoryChannel` to the desired memory channel and `MemChannelClear` to true (1).
2. Read `MemChannelError` to check for errors.

Note

The flash memory (non-volatile memory) of Pike cameras has a minimum of 100 000 write-erase cycles.

Memory channel error codes

ID	Error description
0x00	No error
0x01	Memory detection error

Table 165: Memory channel error description

ID	Error description
0x02	Memory size error
0x03	Memory erase error
0x04	Memory write error
0x05	Memory header write error
0x0F	Memory channel out of range

Table 165: Memory channel error description (continued)

Deferred image transport

Using this register, the sequence of recording and the transfer of the images can be paused. Setting `HoldImg` prevents transfer of the image. The images are stored in `ImageFIFO`.

The images indicated by `NumOfImages` are sent by setting the `SendImage` bit.

When `FastCapture` is set (in Format_7 only), images are recorded at the highest possible frame rate.

Register	Name	Field	Bit	Description
0xF1000260	DEFERRED_TRANS	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 4]	Reserved
		SendImage	[5]	Send NumOfImages now (auto reset)
		HoldImg	[6]	Enable/Disable deferred transport mode
		FastCapture	[7]	Enable/disable fast capture mode
		---	[8 to 15]	Reserved
		FiFoSize	[16 to 23]	Size of FiFo in number of images (read only)
		NumOfImages	[24 to 31]	Write: Number of images to send Read: Number of images in buffer

Table 166: Advanced register: Deferred image transport

Frame information

This register can be used to double-check the number of images received by the host computer against the number of images which were transmitted by the camera. The camera increments this counter with every FrameValid signal. This is a mirror of the frame counter information found at 0xF1000610.

Register	Name	Field	Bit	Description
0xF1000270	FRAMEINFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		ResetFrameCnt	[1]	Reset frame counter
		---	[1 to 31]	Reserved
0xF1000274	FRAMECOUNTER	FrameCounter	[0 to 31]	Number of captured frames since last reset

Table 167: Advanced register: Frame information

The `FrameCounter` is incremented when an image is read out of the sensor.

The `FrameCounter` does not indicate whether an image was sent over the IEEE1394 bus or not.

Input/output pin control

Note

- See Input/output pin control on page 86
- See IO_INP_CTRL 1-2 on page 87
- See IO_OUTP_CTRL 1-4 on page 91
- See Output modes on page 92

Delayed Integration enable

A delay time between initiating exposure on the sensor and the activation edge of the `IntEna` signal can be set using this register. The `on/off` flag activates/deactivates integration delay. The time can be set in µs in `DelayTime`.

Note

- Only one edge is delayed.
- If `IntEna_Out` is used to control an exposure, it is possible to have a variation in brightness or to precisely time a flash.

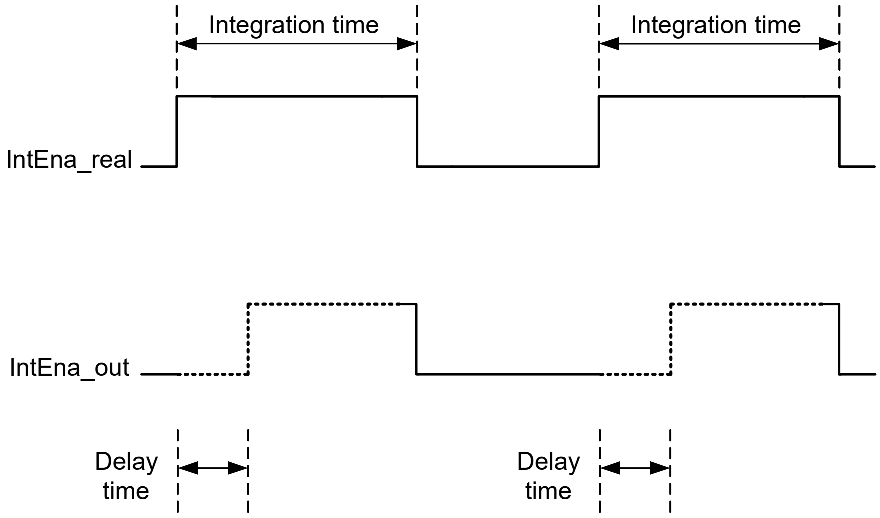


Figure 116: Delayed integration timing

Register	Name	Field	Bit	Description
0xF1000340	IO_INTENA_DELAY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Enable/disable integration enable delay
		---	[7 to 11]	Reserved
		DELAY_TIME	[12 to 31]	Delay time in µs

Table 168: Advanced register: Delayed Integration Enable

Auto shutter control

The table below illustrates the advanced register for `auto shutter control`. The purpose of this register is to limit the range within which auto shutter operates.

Register	Name	Field	Bit	Description
0xF1000360	AUTOSHUTTER_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 31]	Reserved

Table 169: Advanced register: Auto shutter control

Register	Name	Field	Bit	Description
0xF1000364	AUTOSHUTTER_LO	---	[0 to 5]	Reserved
		MinValue	[6 to 31]	Minimum auto shutter value lowest possible value: 10 µs
0xF1000368	AUTOSHUTTER_HI	---	[0 to 5]	Reserved
		MaxValue	[6 to 31]	Maximum auto shutter value

Table 169: Advanced register: Auto shutter control (continued)

Note

- Values can only be changed within the limits of shutter CSR.
- Changes in auto exposure register only have an effect when auto shutter is enabled.
- Auto exposure limits are: 50..205 (`SmartView`→`Ctrl1` `tab`: `Target gray level`)

When both `auto shutter` and `auto gain` are enabled, priority is given to increasing shutter when brightness decreases. This is done to achieve the best image quality with lowest noise.

For increasing brightness, priority is given to lowering gain first for the same purpose.

`MinValue` and `MaxValue` limits the range the auto shutter feature is allowed to use for the regulation process. Both values are initialized with the minimum and maximum value defined in the standard SHUTTER_INQ register (multiplied by the current active timebase).

If you change the `MinValue` and/or `MaxValue` and the new range exceeds the range defined by the SHUTTER_INQ register, the standard SHUTTER register will not show correct shutter values. In this case you should read the EXTENDED_SHUTTER register for the current active shutter time.

Changing the auto shutter range might not affect the regulation, if the regulation is in a stable condition and no other condition affecting the image brightness is changed.

If both `auto gain` and `auto shutter` are enabled and if the shutter is at its upper boundary and gain regulation is in progress, increasing the upper auto shutter boundary has no effect on auto gain/shutter regulation as long as auto gain regulation is active.

Note

As with the Extended Shutter the value of `MinValue` and `MaxValue` must not be set to a lower value than the minimum shutter time.

Auto gain control

The table below illustrates the advanced register for `auto gain control`.

Register	Name	Field	Bit	Description
0xF1000370	AUTOGAIN_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 3]	Reserved
		MaxValue	[4 to 15]	Maximum auto gain value
		---	[16 to 19]	Reserved
		MinValue	[20 to 31]	Minimum auto gain value

Table 170: Advanced register: Auto gain control

`MinValue` and `MaxValue` limits the range the auto gain feature is allowed to use for the regulation process. Both values are initialized with the minimum and maximum value defined in the standard GAIN_INQ register.

Changing the `auto gain range` might not affect the regulation, if the regulation is in a stable condition and no other condition affecting the image brightness is changed.

If both `auto gain` and `auto shutter` are enabled and if the gain is at its lower boundary and shutter regulation is in progress, decreasing the lower auto gain boundary has no effect on auto gain/shutter regulation as long as auto shutter regulation is active.

Both values can only be changed within the range defined by the standard GAIN_INQ register.

Autofunction AOI

The table below illustrates the advanced register for `autofunction AOI`.

Register	Name	Field	Bit	Description
0xF1000390	AUTOFNC_AOI	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 3]	Reserved
		ShowWorkArea	[4]	Show work area
		---	[5]	Reserved
		ON_OFF	[6]	Enable/disable AOI (see note above)
		---	[7]	Reserved
		YUNITS	[8 to 19]	Y units of work area/pos. beginning with 0 (read only)
		XUNITS	[20 to 31]	X units of work area/pos. beginning with 0 (read only)
0xF1000394	AF_AREA_POSITION	Left	[0 to 15]	Work area position (left coordinate)
		Top	[16 to 31]	Work area position (top coordinate)
0xF1000398	AF_AREA_SIZE	Width	[0 to 15]	Width of work area size
		Height	[16 to 31]	Height of work area size

Table 171: Advanced register: Autofunction AOI

The possible increment of the work area position and size is defined by the YUNITS and XUNITS fields. The camera automatically adjusts your settings to permitted values.

Note

If the adjustment fails and the work area size and/or work area position becomes invalid, then this feature is automatically switched off.

Read back the ON_OFF flag, if this feature does not work as expected.

Color correction

To switch off color correction in YUV mode, see bit [6]

Register	Name	Field	Bit	Description
0xF10003A0	COLOR_CORR	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Color correction on/off default: on Write: 02000000h to switch color correction OFF Write: 00000000h to switch color correction ON
		Reset	[7]	Reset to defaults
		---	[8 to 31]	Reserved
0xF10003A4	COLOR_CORR_COEFFIC11 = Crr		[0 to 31]	A number of 1000 equals a color correction coefficient of 1. Color correction values range -1000..+2000 and are signed 32 bit. In order for white balance to work properly ensure that the row sum equals to 1000. The maximum row sum is limited to 2000.
0xF10003A8	COLOR_CORR_COEFFIC12 = Cgr		[0 to 31]	
0xF10003AC	COLOR_CORR_COEFFIC13 = Cbr		[0 to 31]	
0xF10003B0	COLOR_CORR_COEFFIC21 = Crg		[0 to 31]	
0xF10003B4	COLOR_CORR_COEFFIC22 = Cgg		[0 to 31]	
0xF10003B8	COLOR_CORR_COEFFIC23 = Cbg		[0 to 31]	
0xF10003BC	COLOR_CORR_COEFFIC31 = Crb		[0 to 31]	
0xF10003C0	COLOR_CORR_COEFFIC32 = Cgb		[0 to 31]	
0xF10003C4	COLOR_CORR_COEFFIC33 = Cbb		[0 to 31]	
0xF10003A4 ... 0xF10003FC				Reserved for testing purposes do not touch!

Table 172: Advanced register: Color correction

For an explanation of the color correction matrix and for further information read Color correction on page 166.

Trigger delay

Register	Name	Field	Bit	Description
0xF1000400	TRIGGER_DELAY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Trigger delay on/off
		---	[7 to 10]	Reserved
		DelayTime	[11 to 31]	Delay time in µs

Table 173: Advanced register: Trigger delay

The advanced register allows start of the integration to be delayed via `DelayTime` by maximum 2^{21} µs, which is maximum 2.1 s after a trigger edge was detected.

Note Trigger delay works with external trigger modes only.

Mirror image

The table below illustrates the advanced register for `Mirror image`.

Register	Name	Field	Bit	Description
0xF1000410	MIRROR_IMAGE	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Mirror image on/off 1: on 0: off Default: off
		---	[7 to 31]	Reserved

Table 174: Advanced register: Mirror image

AFE channel compensation (channel balance)

All ON Semiconductor Pike sensors are read out via two channels: the first channel for the left half of the image and the second channel for the right half of the image.

Channel gain adjustment (Pike color cameras: only RAW8 and RAW16) for both channels can be done via the following two advanced registers:

Register	Name	Field	Bit	Description
0xF1000420	ADV_CHN_ADJ_GAIN	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 31]	Reserved
0xF1000424	ADV_CHN_ADJ_GAIN	---	[0 to 15]	Reserved
		Gain_Value	[16 to 31]	Signed 16-bit value -8192 to 0 to +8191 SmartView shows only: -2048 to 0 to +2047

Table 175: Advanced register: Channel balance

You can save the current value in the user sets and set to default value.

Dual-tap offset adjustment

(only for the following Pike cameras having ON Semiconductor/Sony Semiconductor sensors with two channels: Pike F-032, Pike F-210, Pike F-421, Pike F-505, Pike F-1100, Pike F-1600)

For fine tuning of both channels a so-called dual-tap offset adjustment is possible: in addition to channel gain adjustment also an offset adjustment can be done. This will lead to a (nearly) perfect channel compensation for all gray values.

Offset adjustment (Pike color cameras: only RAW8 and RAW16) for both channels can be done via the following two advanced registers.

Register	Name	Field	Bit	Description
0xF1000430	ADV_CHN_ADJ_OFFSET	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 31]	Reserved

Table 176: Advanced register: Dual-tap offset adjustment

Register	Name	Field	Bit	Description
0xF1000434	ADV_CHN_ADJ_OFFSET+1	---	[0 to 15]	Reserved
		Offset_Value	[16 to 31]	Signed 16-bit value -255 to 0 to +256 SmartView shows only: -255 to 0 to +255 Note: Direct register access. up to +256 whereas SmartView: up to +255)

Table 176: Advanced register: Dual-tap offset adjustment (continued)

You can save the current value in the user sets and set to default value.

Note

Doing the dual-tap offset adjustment in SmartView: Refer to the FirePackage/FirePackage64 *SmartView Manual.*

Soft reset

Register	Name	Field	Bit	Description
0xF1000510	SOFT_RESET	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		Reset	[6]	Initiate reset
		---	[7 to 19]	Reserved
		Delay	[20 to 31]	Delay reset in 10 ms steps

Table 177: Advanced register: Soft reset

The `soft reset` feature is similar to the INITIALIZE register, with the following differences:

- 1 or more bus resets will occur
- the FPGA will be rebooted

The reset can be delayed by setting the `Delay` to a value unequal to 0.

The delay is defined in 10 ms steps.

Note

When SOFT_RESET has been defined, the camera will respond to further read or write requests but will not process them.

High SNR mode (High Signal Noise Ratio)

With `High SNR` mode enabled the camera internally grabs `GrabCount` images and outputs a single averaged image.

Register	Name	Field	Bit	Description
0xF1000520	HIGH_SNR	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	High SNR mode on/off The camera must be idle to toggle this feature on/off. Idle means: no image acquisition, no trigger. Set grab count and activation of HighSNR in `one single write access`.
		---	[7 to 22]	Reserved
		GrabCount	[23 to 31]	Number of images (min. 2) 2^n images with n=1..8 (automatically)

Table 178: Advanced register: High Signal Noise Ratio (HSNR)

Note

- The camera must be idle to toggle this feature on/off. Idle means: no image acquisition, no trigger.
- Set grab count and activation of HighSNR in `one single write access`.

Maximum ISO packet size

Use this feature to increase the MaxBytePerPacket value of Format_7 modes. This overrides the maximum allowed isochronous packet size specified by IIDC V1.31.

Register	Name	Field	Bit	Description
0xF1000560	ISOSIZE_S400	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Enable/Disable S400 settings
		Set2Max	[7]	Set to maximum supported packet size
		---	[8 to 15]	Reserved
		MaxIsoSize	[16 to 31]	Maximum ISO packet size for S400
0xF1000564	ISOSIZE_S800	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Enable/Disable S800 settings
		Set2Max	[7]	Set to maximum supported packet size
		---	[8 to 15]	Reserved
		MaxIsoSize	[16 to 31]	Maximum ISO packet size for S800

Table 179: Advanced register: Maximum ISO packet size

Example

For isochronous packets at a speed of S800 the maximum allowed packet size (IIDC V1.31) is 8192 byte. This feature allows you to extend the size of an isochronous packet up to 11.000 byte at S800. Thus the isochronous bandwidth is increased from 64 MByte/s to approximately 84 MByte/s. You need either PCI Express.

The `Maximum ISO packet size` feature ...

- ... reduces the asynchronous bandwidth available for controlling cameras by approximately 75%
- ... may lead to slower responses on commands
- ... is not covered by the IEEE1394 specification
- ... may not work with all available IEEE1394 host adapters.

Note

We strongly recommend to use `PCI Express` adapter.

Restrictions

Note the restrictions in the following table. When using software with an Isochronous Resource Manager (IRM): deactivate it.

Software	Restrictions
FireGrab	Deactivate Isochronous Resource Manager: SetParameter (FGP_USEIRMFORBW, 0)
FireStack/FireClass	No restrictions
SDKs using Microsoft driver (Active FirePackage, Direct FirePackage, ...)	n/a
Linux: libdc1394_1.x	No restrictions
Linux: libdc1394_2.x	Deactivate Isochronous Resource Manager: Set DC1394_CAPTURE_FLAGS_BANDWIDTH_ALLOC flag to 0
Third Party Software	Deactivate Isochronous Resource Manager

Table 180: Restrictions for feature: Maximum ISO packet size

Operation The maximum allowed isochronous packet size can be set separately for the ISO speeds S400 and S800. Check the associated `Presence_Inq` flag to see for which ISO speed this feature is available.

Setting the `Set2Max` flag to 1 sets the `MaxIsoSize` field to the maximum supported isochronous packet size. Use this flag to query the maximum supported size (may depend on the camera model).

Enable this feature by setting the `ON_OFF` flag to 1 and the `MaxIsoSize` field to a value greater than the default packet size.

The camera ensures:

- that the value of the `MaxIsoSize` field is a multiple of 4.
- that the value is not lower than the value specified by the IEEE1394 specification.

The settings are stored in the user sets.

Note

Enabling this feature will not change the `MaxBytePerPacket` value automatically. The camera may not use the new isochronous packet size for the `MaxBytePerPacket` value until a write access to the desired Format_7 mode has been issued.

Quick parameter change timing modes

You can choose between the following update timing modes:

- **Standard Parameter Update Timing** (slightly modified from previous Pike cameras)
- New: **Quick Format Change Mode**

Note

For a detailed description see Quick parameter change timing modes on page 153.

Register	Name	Field	Bit	Description
0xF1000570	PARAMUPD_TIMING	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		UpdActive	[6]	Update active See **Encapsulated Update (begin/ end)** on page 155 0: (default); reset to 0 means `Encapsulated Update end` 1: set to 1 means `Encapsulated Update begin`
		---	[7 to 23]	Reserved
		UpdTiming	[24 to 31]	Update timing mode If set to O: **Standard Parameter Update Timing** is active If set to 2: **Quick Format Change Mode** is active

Table 181: Advanced register: Update timing modes

Standard Parameter Update Timing

The camera behaves like older firmware versions without this feature. The `UpdActive` flag has no meaning.

Quick Format Change Mode

This mode behaves like **Standard Parameter Update Timing** mode with the following exception:

An already started image transport to the host will not be interrupted, but an already started integration will be interrupted.

To switch on **Quick Format Change Mode** do the following:

1. Set UpdTiming to 2.
2. Set UpdActive to 1.
3. Be aware that all parameter values have to be set within 10 seconds.

Automatic reset of the UpdActive flag

With **Quick Format Change Mode** you normally have to clear the `UpdActive` flag after all desired parameters have been set. Every time the `PARAMUPD_TIMING` register is written to with the `UpdActive` flag set to 1 a 10 second time-out is started / restarted. If the time-out passes before you clear the `UpdActive` flag, the `UpdActive` flag is cleared automatically and all parameter changes since setting the `UpdActive` flag to 1 become active automatically.

Low-noise binning mode (only 2 × H-binning)

This register enables/disables low-noise binning mode.

This means: an average (and not a sum) of the luminance values is calculated within the FPGA.

The image is therefore darker than with the usual binning mode, but the signal-to-noise ratio is better (approximately a factor of $\sqrt{2}$) than without binning.

Offset	Name	Field	Bit	Description
0xF10005B0	LOW_NOISE_BINNING	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Low-noise binning mode on/off
		---	[7 to 31]	Reserved

Table 182: Advanced register: Low-noise binning mode

Software feature control (disable LEDs / switch single-tap and dual-tap)

The software feature control register allows to enable or disable some features of the camera (e.g. disable LEDs or switch single-tap and dual-tap for Pike F-1100, F-1600). The settings are stored permanently within the camera and do not depend on any user set.

Register	Name	Field	Bit	Description
0xF1000640	SWFEATURE_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		BlankLED_Inq	[1]	Indicates presence of *Disable LEDs* feature.
		DigitizationTaps_Inq	[2]	Indicates presence of *Sensor digitization taps* feature.
		---	[3 to 5]	Reserved
		SensorTaps_Inq	[6]	Indicates presence of *Sensor taps* feature.
		---	[7 to 15]	Reserved
		---	[16]	Reserved
		BlankLED	[17]	0: Behavior as described in Status LEDs on page 84. 1: Disable LEDs. (Only error codes are shown.)
		DigitizationTaps	[18 to 21]	0: single-tap 1: dual-tap
		SensorTaps	[22 to 25]	Max number of taps-1
		---	[26 to 31]	Reserved

Table 183: Advanced register: Software feature control (disable LEDs/switch single-tap and dual-tap)

Disable LEDs

- To disable LEDs set bit [17] to 1.
- To disable LEDs in SmartView:
  `Adv3` tab, activate *Disable LED functionality* check box.

The camera does not show any more the status indicators during normal operation:

Examples:

- Power on is not shown
- Isochronous traffic is not shown
- Asynchronous traffic is not shown

Note

During the startup of the camera and if an error condition is present, the LEDs behave as described in Status LEDs on page 84.

Sensor digitization taps (Pike F-1100, F-1600 only)

The sensor digitization taps fields `DigitizationTaps` [18 to 21] and `SensorTaps` [22 to 25] allow to switch between single-tap and dual-tap mode of a multi-tap sensor (Pike F-1100, F-1600). The settings are stored permanently within the camera and do not depend on any user set.

- To switch single-tap set bit [18 to 21] to 0.
- To switch dual-tap set bit [18 to 21] to 1.

Note

After switching the number of tabs reboot the camera by releasing a SoftReset.

- To get info how many taps are present read out bit [22 to 25].
  – 0 indicates 1 tap.
  – 1 indicates 2 taps.

Parameter-List Update

The parameter list is an array of address/data pairs which can be sent to the camera in a single bus cycle.

Register	Name	Field	Bit	Description
0xF1100000	PARAMLIST_INFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 15]	Reserved
		BufferSize	[16 to 31]	Size of parameter list buffer in bytes
0xF1101000 ... 0xF1101nnn	PARAMLIST_BUFFER			

Table 184: Advanced register: **Parameter-List Update***: parameter list*

Dependant on the parameter update mode the address/data pairs may become active one by one or after the processing of the complete parameter list. A parameter list may look like follows (the description is for your convenience):

Address offset	Data quadlet	Description
0xF0F00608	0xE0000000	Set video format 7
0xF0F00604	0x00000000	Set video mode 0
0xF0F08008	0x00000000	Set image position
0xF0F0800C	0x028001E0	Set image size
0xF0F08044	0x04840484	Set BytePerPacket value
0xF0F0080C	0x80000100	Set shutter to 0x100
0xF0F00820	0x80000080	Set gain to 0x80

Table 185: Example: parameter list

Note

- The PARAMLIST_BUFFER shares the memory with the GPDATA_BUFFER. Therefore it is not possible to use both features at the same time.
- Not all CSRs or features of a particular camera model can be used with the parameter list feature.

Format_7 mode mapping

With Format_7 mode mapping it is possible to map special binning and sub-sampling modes to F7M1 to F7M7 (see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152).

Register	Name	Field	Bit	Description
0xF1000580	F7MODE_MAPPING	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 31]	Reserved
0xF1000584	F7MODE_MAP_INQ	F7MODE_00_INQ	[0]	Format_7 Mode_0 presence
		F7MODE_01_INQ	[1]	Format_7 Mode_1 presence
		...	...	...
		F7MODE_31_INQ	[31]	Format_7 Mode_31 presence
0xF1000588	Reserved	---	---	---
0xF100058C	Reserved	---	---	---
0xF1000590	F7MODE_0	Format_ID	[0 to 31]	Format ID (read only)
0xF1000594	F7MODE_1	Format_ID	[0 to 31]	Format ID for Format_7 Mode_1
0xF1000598	F7MODE_2	Format_ID	[0 to 31]	Format ID for Format_7 Mode_2
0xF100059C	F7MODE_3	Format_ID	[0 to 31]	Format ID for Format_7 Mode_3

Table 186: Advanced register: Format_7 mode mapping

Register	Name	Field	Bit	Description
0xF10005A0	F7MODE_4	Format_ID	[0 to 31]	Format ID for Format_7 Mode_4
0xF10005A4	F7MODE_5	Format_ID	[0 to 31]	Format ID for Format_7 Mode_5
0xF10005A8	F7MODE_6	Format_ID	[0 to 31]	Format ID for Format_7 Mode_6
0xF10005AC	F7MODE_7	Format_ID	[0 to 31]	Format ID for Format_7 Mode_7

Table 186: Advanced register: Format_7 mode mapping (continued)

Additional Format_7 modes

Firmware 3.x adds additional Format_7 modes. Now you can add some special Format_7 modes which are not covered by the IIDC standard. These special modes implement `binning` and `sub-sampling`.

To stay as close as possible to the IIDC standard the Format_7 modes can be mapped into the register space of the standard Format_7 modes.

There are visible Format_7 modes and internal Format_7 modes:

- At any time only 8 Format_7 modes can be accessed by a host computer.
- Visible Format_7 modes are numbered from 0 to 7.
- Internal Format_7 modes are numbered from 0 to 31.

Format_7 Mode_0 represents the mode with the maximum resolution of the camera: this visible mode cannot be mapped to any other internal mode.

The remaining visible Format_7 Mode_1 ... Mode_7 can be mapped to any internal Format_7 mode.

Example

To map the internal Format_7 Mode_19 to the visible Format_7 Mode_1, write the decimal number 19 to the above listed F7MODE_1 register.

Note

For available Format_7 modes see Figure 70: Mapping of possible Format_7 modes to F7M1 to F7M7 on page 152.

Setting the F7MODE_x register to:

- -1 forces the camera to use the factory defined mode
- -2 disables the respective Format_7 mode (no mapping is applied)

After setup of personal Format_7 mode mappings you have to reset the camera. The mapping is performed during the camera startup only.

Secure image signature (SIS)

Secure image signature (SIS) is the synonym for data, which is inserted into an image to improve or check image integrity.

All Pike models can insert

- `Time stamp` (IEEE1394 bus cycle time at the beginning of integration)

- Frame counter (frames read out of the sensor)
- Trigger counter (external trigger seen only)
- Various camera settings

into a selectable line position within the image. Frame counter and trigger counter are available as advanced registers to be read out directly.

Advanced register: SIS

The SIS feature is controlled by the following advanced feature register:

Note

This register is different to the Marlin time stamp (600) register!

Register	Name	Field	Bit	Description
0xF1000630	SIS	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	SIS mode on/off
		---	[7 to 15]	Reserved
		LineNo	[16 to 31]	SIS data position inside an image
0xF1000634		UserValue	[0 to 31]	User provided value for sequence mode to be placed into the SIS area of an image

Table 187: Advanced register: secure image signature (SIS)

Enabling this feature, SIS data will be inserted into any captured image. The size of SIS data depends on the selected SIS format.

The LineNo field indicates at which line the SIS data will be inserted.

Enter a

- positive value from 0..HeightOfImage to specify a position relative to the top of the image. LinePos=0 specifies the very first image line.
- negative value from-1..-HeightOfImage to specify a position relative to the bottom of the image. LinePos=-1 specifies the very last image line.

SIS UserValue can be written into the camera's image. In sequence mode for every sequence entry an own SIS UserValue can be written.

Note

SIS outside the visible image area:

For certain Format_7 modes the image frame transported may contain padding (filling) data at the end of the transported frame. Setting LinePos=HeightOfImage places the stamp in this padding data area, outside the visible area (invisible SIS).

If the transported image frame does not contain any padding data the camera will not relocate the SIS to the visible area automatically (no SIS).

Take in mind that the accuracy of the time stamp might be affected by asynchronous traffic – mainly if image settings are changed.

Note

The IEEE1394 cycle counter (aka time stamp) will be inserted into the very first 4 bytes/pixels of a line.

Cycle offset	Cycles	Seconds
Cycle offset 12 bit	Cycle count 13 bit	Second count 7 bit
0 to 3071 cycle offsets (40.69 ns)	0 to 7999 cycles	0 to 127 seconds
24.576 MHz cycle timer counter	8000 Hz cycle timer counter	1 Hz cycle timer counter

Table 188: 32-bit cycle timer layout

<table>
<tr><td>Bit</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td></tr>
<tr><td></td><td colspan="12">Cycle offset 12 bit</td><td colspan="4">Cycle count ...</td></tr>
</table>

<table>
<tr><td>Bit</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td></td><td colspan="9">... Cycle count 13 bit</td><td colspan="7">Second count 7 bit</td></tr>
</table>

Table 189: Cycle timer layout

Advanced register: frame counter

Note

Different to Marlin SIS:

Register 610 is only to be used to reset the frame counter.

The frame counter feature is controlled by the following advanced feature register:

Register	Name	Field	Bit	Description
0xF1000610	FRMCNT_STAMP	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Reset	[1]	Reset frame counter
		---	[2 to 31]	Reserved
0xF1000614	FRMCNT		[0 to 31]	Frame counter

Table 190: Advanced register: Frame counter

Having this feature enabled, the current `frame counter` value (images read out of the sensor, equivalent to # FrameValid) will be inserted as a 32-bit integer value into any captured image.

Setting the `Reset` flag to 1 resets the frame counter to 0: the `Reset` flag is self-cleared.

Note

The 4 bytes of the frame counter value will be inserted as the 5th to 8th byte of a line.

Additionally there is a register for direct read out of the frame counter value.

Advanced register: trigger counter

The trigger counter feature is controlled by the following advanced feature register:

Register	Name	Field	Bit	Description
0xF1000620	TRIGGER_COUNTER	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Reset	[1]	Reset trigger counter
		---	[2 to 31]	Reserved
0xF1000624	TRGCNT	TriggerCounter	[0 to 31]	Trigger counter

Table 191: Advanced register: Trigger counter

Having this feature enabled, the current `trigger counter` value (external trigger seen by hardware) will be inserted as a 32-bit integer value into any captured image.

Setting the `Reset` flag to 1 resets the `trigger counter` to 0: the Reset flag is self-cleared.

The `ON_OFF` and `LinePos` fields are simply mirrors of the time stamp feature. Settings of these fields are applied to all image stamp features.

Note

The four bytes of the trigger counter value will be inserted as the 9th to 12th byte of a line.

Additionally there is a register for direct read out of the `trigger counter` value.

Where to find time stamp, frame counter and trigger counter in the image

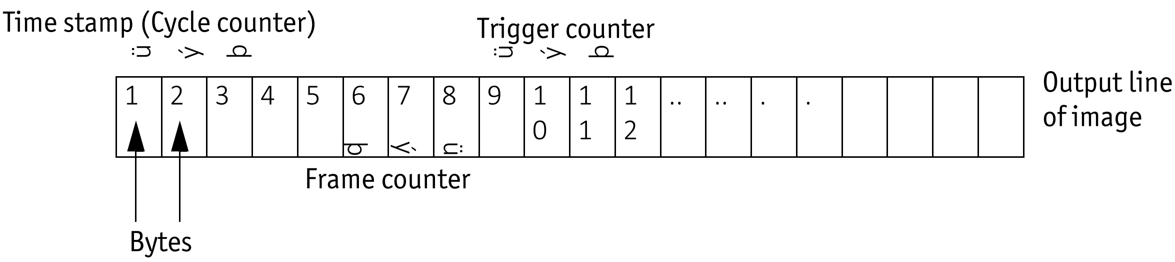


Figure 117: SIS in the image: time stamp, frame counter, trigger counter

Where to find all SIS values in the image

In the following table you find the position of all SIS values (byte for byte) including the endianness of SIS values.

CycleCounter [7 to 0]	CycleCounter [15 to 8]	CycleCounter [23 to 16]	CycleCounter [31 to 24]
Byte 1	Byte 2	Byte 3	Byte 4
FrameCounter [7 to 0]	FrameCounter [15 to 8]	FrameCounter [23 to 16]	FrameCounter [31 to 24]
Byte 5	Byte 6	Byte 7	Byte 8
TriggerCounter [7 to 0]	TriggerCounter [15 to 8]	TriggerCounter [23 to 16]	TriggerCounter [31 to 24]
Byte 9	Byte 10	Byte 11	Byte 12
AoiLeft [7 to 0]	AoiLeft [15 to 8]	AoiTop [7 to 0]	AoiTop [15 to 8]
Byte 13	Byte 14	Byte 15	Byte 16
AoiWidth [7 to 0]	AoiWidth [15 to 8]	AoiHeight [7 to 0]	AoiHeight [15 to 8]
Byte 17	Byte 18	Byte 19	Byte 20
Shutter [7 to 0]	Shutter [15 to 8]	Shutter [23 to 16]	Shutter [31 to 24]
Byte 21	Byte 22	Byte 23	Byte 24
Gain [7 to 0]	Gain [15 to 8]	Reserved [NULL]	Reserved [NULL]
Byte 25	Byte 26	Byte 27	Byte 28
OutputState_1 [7 to 0]	OutputState_2 [7 to 0]	OutputState_3 [7 to 0]	OutputState_4 [7 to 0]
Byte 29	Byte 30	Byte 31	Byte 32
InputState_1 [7 to 0]	InputState_2 [7 to 0]	Reserved [NULL]	Reserved [NULL]
Byte 33	Byte 34	Byte 35	Byte 36
SequenceIndex [7 to 0]	Reserved [NULL]	ColorCoding [NULL]	Reserved [NULL]
Byte 37	Byte 38	Byte 39	Byte 40
SerialNumber [7 to 0]	SerialNumber [15 to 8]	SerialNumber [23 to 16]	SerialNumber [31 to 24]
Byte 41	Byte 42	Byte 43	Byte 44
SIS_UserValue [7 to 0]	SIS_UserValue [15 to 8]	SIS_UserValue [23 to 16]	SIS_UserValue [31 to 24]
Byte45	Byte46	Byte47	Byte48

Table 192: SIS values (increasing order of transmitted pixels)

Smear reduction (not Pike F-1100, F-1600)

To enable or disable smear reduction use the following register(s):

Register	Name	Field	Bit	Description
0xF1000440	`LOW_SMEAR`	`Presence_Inq`	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Smear reduction on/off
		---	[7 to 31]	Reserved

Table 193: Advanced register: Smear reduction

Defect pixel correction

In the following the abbreviation DPC for Defect Pixel Correction will be used.

To enable or disable and configure defect pixel correction use the following register(s):

Register	Name	Field	Bit	Description
0xF1000460	DEFECT_PIXEL_CORRECTION_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		ON_OFF	[6]	Defect pixel correction (DPC) on/off
		---	[7 to 31]	Reserved
0xF1000464	DEFECT_PIXEL_CORRECTION_MEM	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1]	Reserved
		EnaMemWR	[2]	Enable WR access (from host to µC)
		EnaMemRD	[3]	Enable RD access (from µC to host)
		---	[4 to 9]	Reserved
		Number DefectColumn	[10 to 17]	Number of current defect columns (6 byte / column)
		Number DefectPixel	[18 to 31]	Number of current defect pixels (4 byte / pixel)
0xF1000468	DEFECT_PIXEL_CORRECTION_INFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Version	[1 to 3]	Feature version
		---	[4 to 19]	reserved
		MaxDPCTable Size	[20 to 31]	Maximum size of DPC table (in 128 Byte Blocks)

Table 194: Advanced register: Defect pixel correction

Reading or writing defect pixel correction data from/into the camera

Accessing the defect pixel correction data inside the camera is done through the GPDATA_BUFFER. Because the size of the GPDATA_BUFFER is smaller than the whole defect pixel correction data the data must be written in multiple steps.

Defect pixels and columns are saved in two adjacent memory chunks, first the defect pixel chunk followed by defect columns.

DPC-Memory alignment: {defect_pixel_1, defect_pixel_2 to defect_pixel_n, defect_column_1, defect_column_2 to defect_column_n}.

One defect pixel is saved as two 16-bit values (X, Y), so the size of defect pixel chunk equals `NumberDefectPixel` * 4 (it is also the offset of defect column data).

One defect column is saved as three 16-bit values (X, Y, Height), so the size of defect column chunk equals `NumberDefectColumn` * 6

Note

Pixel coordinates and column coordinates must be sorted ascending, by X as primary and Y as secondary sorting-key.

To write DPC coordinates:

1. Query the limits and ranges by reading `DEFECT_PIXEL_CORRECTION_INFO` and `GPDATA_INFO`.
   (Note: If the list is empty, you do not have to write the DPC pixels. In this case do the following: in `DEFECT_PIXEL_CORRECTION_MEM` set the `NumberDefectColumn` and `NumberDefectPixel` to 0.)
2. Set `EnableMemWR` to true (1).
3. Update `NumberDefectColumn` and `NumberDefectPixel` in `DEFECT_PIXEL_CORRECTION_MEM` to the new values.
4. Write n DPC data bytes to `GPDATA_BUFFER` (n might be lower than the size of the `GPDATA_BUFFER`)
5. Repeat step 4 until all data is transferred.
6. Set `EnableMemWR` to false.

To read a DPC coordinates:

1. Query the limits and ranges by reading `DEFECT_PIXEL_CORRECTION_INFO and GPDATA_INFO`.
2. Query `NumberDefectColumn` and `NumberDefectPixel` from `DEFECT_PIXEL_CORRECTION_MEM`
3. Set `EnableMemRD` to true (1).
4. Read n DPC data bytes from `GPDATA_BUFFER` (n might be lower than the size of the `GPDATA_BUFFER`).
5. Repeat step 4 until all data is transferred.
6. Set EnableMemRD to false.

User profiles

Definition

Within the IIDC specification user profiles are called memory channels. Often they are called user sets. In fact these are different expressions for the following: storing camera settings into a non-volatile memory inside the camera.

User profiles can be programmed with the following advanced feature register:

Offset	Name	Field	Bit	Description
0xF1000550	USER_PROFILE	Presence_Inq	[0]	Indicates presence of this feature (read only)
		Error	[1]	An error occurred
		---	[2 to 6]	Reserved
		Busy	[7]	Save/Load in progress
		Save	[8]	Save settings to profile
		Load	[9]	Load settings from profile
		SetDefaultID	[10]	Set Profile ID as default
		---	[11 to 19]	Reserved
		ErrorCode	[20 to 23]	Error code See Table 196: User profiles: Error codes on page 332.
		---	[24 to 27]	Reserved
		ProfileID	[28 to 31]	ProfileID (memory channel)

Table 195: Advanced register: User profiles

In general this advanced register is a wrapper around the standard memory channel registers with some extensions. So to query the number of available user profiles you have to check the Memory_Channel field of the BASIC_FUNC_INQ register at offset 0x400 (see IIDC V1.31 for details).

The ProfileID is equivalent to the memory channel number and specifies the profile number to store settings to or to restore settings from. In any case profile #0 is the hard-coded factory profile and cannot be overwritten.

After an initialization command, startup or reset of the camera, the ProfileID also indicates which profile was loaded on startup, reset or initialization.

Note

- The default profile is the profile that is loaded on power-up or an INITIALIZE command.
- A save or load operation delays the response of the camera until the operation is completed. At a time only one operation can be performed.

Store — To store the current camera settings into a profile:

1. Write the desired ProfileID with the SaveProfile flag set.
2. Read back the register and check the ErrorCode field.

Restore — To restore the settings from a previous stored profile:

1. Write the desired `ProfileID` with the `RestoreProfile` flag set.
2. Read back the register and check the `ErrorCode` field.

Set default — To set the default profile to be loaded on startup, reset or initialization

1. Write the desired `ProfileID` with the `SetDefaultID` flag set.
2. Read back the register and check the `ErrorCode` field.

Error codes

Error Code	Description
0x00	No error
0x01	Profile data corrupted
0x02	Camera not idle during restore operation
0x03	Feature not available (feature not present)
0x04	Profile does not exist
0x05	ProfileID out of range
0x06	Restoring the default profile failed
0x07	Loading LUT data failed
0x08	Storing LUT data failed

Table 196: User profiles: Error codes

Reset of error codes

The `ErrorCode` field is set to zero on the next write access.

You may also reset the `ErrorCode`

- by writing to the `USER_PROFILE` register with the `SaveProfile`, `RestoreProfile` and `SetDefaultID` flag not set.
- by writing `00000000h` to the `USER_PROFILE` register.

Stored settings

The following table shows the settings stored inside a profile:

Standard registers	Standard registers (Format_7)	Advanced registers
Cur_V_Frm_Rate Cur_V_Mode Cur_V_Format ISO_Channel ISO_Speed BRIGHTNESS AUTO_EXPOSURE (Target gray level) SHARPNESS WHITE_BALANCE (+ auto on/off) HUE (+ hue on) SATURATION (+ saturation on) GAMMA (+ gamma on) SHUTTER (+ auto on/off) GAIN TRIGGER_MODE TRIGGER_POLARITY TRIGGER_DELAY ABS_GAIN	IMAGE_POSITION (AOI) IMAGE_SIZE (AOI) COLOR_CODING_ID BYTES_PER_PACKET	TIMEBASE EXTD_SHUTTER IO_INP_CTRL IO_OUTP_CTRL IO_INTENA_DELAY AUTOSHUTTER_CTRL AUTOSHUTTER_LO AUTOSHUTTER_HI AUTOGAIN_CTRL AUTOFNC_AOI (+ on/off) COLOR_CORR (on/off + color correction coefficients) TRIGGER_DELAY MIRROR_IMAGE HIGH_SNR LUT_CTRL (LutNo; ON_OFF is not saved; up to 16 LUTs can be saved in four user sets) SHDG_CTRL (on/off + ShowImage) DEFERRED_TRANS (HoldImg + NumOfImages) CHANNEL_ADJUST_CTRL CHANNEL_ADJUST_VALUE ADV_CHN_ADJ_OFFSET ADV_CHN_ADJ_OFFSET+1

Table 197: User profile: stored settings

The user can specify which user profile will be loaded upon startup of the camera.

This frees the user software from having to restore camera settings, that differ from default, after every cold start. This can be especially helpful if third party software is used which may not give easy access to certain advanced features or may not provide efficient commands for quick writing of data blocks into the camera.

Note

- A profile save operation automatically disables capturing of images.
- A profile save or restore operation is an uninterrupted (atomic) operation. The write response (of the asynchronous write cycle) will be sent after completion of the operation.
- Restoring a profile will not overwrite other settings than listed above.
- If a restore operation fails or the specified profile does not exist, all registers will be overwritten with the hard-coded factory defaults (profile `#0`).
- Data written to this register will not be reflected in the standard memory channel registers.

Frame time control

With this register you can set the frame time (in microseconds) and thus control the sensor frame rate more precisely than with the `BytesPerPacket` settings.

Note

- The image transport speed depends on the `BytesPerPacket` setting only.
- The camera corrects invalid values automatically.

Offset	Name	Field	Bit	Description
0xF1000A00	FRAMETIME_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 5]	Reserved
		OnOff	[6]	Enables or disables frame rate control
		---	[7]	Reserved
		FrameTime	[8 to 31]	Frame time in microsecond steps
0xF1000A04		MinValue	[0 to 31]	Minimum frame time
0xF1000A08		MaxValue	[0 to 32]	Maximum frame time

Table 198: Advanced register: Frame time control

- The precision of the frame rate depends on the jitter at start of exposure, see Jitter at start of exposure on page 189.
- The frame rate is affected by both: current shutter time and `BytesPerPacket` setting.

- The FRAMETIME_CTRL register does not change the shutter or BytePerPacket settings.

GPDATA_BUFFER

GPDATA_BUFFER is a general purpose register that regulates the exchange of data between camera and host for:

- writing look-up tables (LUTs) into the camera
- uploading/downloading of the shading image

GPDATA_INFO Buffer size query

GPDATA_BUFFER indicates the actual storage range

Register	Name	Field	Bit	Description
0xF1000FFC	GPDATA_INFO	---	[0 to 15]	Reserved
		BufferSize	[16 to 31]	Size of GPDATA_BUFFER (byte)
0xF1001000 … 0xF10017FC	GPDATA_BUFFER			

Table 199: Advanced register: GPData buffer

Note

- Read the BufferSize before using
- GPDATA_BUFFER can be used by only one function at a time.

Little endian vs. big endian byte order

- Read/WriteBlock accesses to GPDATA_BUFFER are recommended, to read or write more than 4 byte data. This increases the transfer speed compared to accessing every single quadlet.
- The big endian byte order of the IEEE1394 bus is unlike the little endian byte order of common operating systems (Intel PC). Each quadlet of the local buffer, containing the LUT data or shading image for instance, has to be swapped bytewise from little endian byte order to big endian byte order before writing on the bus.

Bit depth	little endian⇨big endian	Description
8 bit	L0 L1 L2 L3⇨L3 L2 L1 L0	L: low byte
16 bit	L0 H0 L1 H1⇨H1 L1 H0 L0	H: high byte

Table 200: Swapped first quadlet at address offset 0

User adjustable gain references

This register gives the user the possibility (via direct access) to modify the gain references. Modified values are stored automatically without further user action and are also stored on restart.

To reload default gain references (which are programmed at personalization) within the camera: set flag `m_bDefGainRef=1`

Offset	Name	Field	Bit	Description
0xF1002000	AFEREFERENCES	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1 to 4]	Reserved
		`m_bDefGainRef`	[5]	Reload default gain references, if this flag is set.
		---	[6 to 31]	Reserved
0xF1002004	GAINREFERENCE	`m_GainRef`	[0 to 31]	Gain reference (0 to 511)

Table 201: Advanced register: User adjustable gain references

In the following table you find the default gain references of all Pike models.

Model	Default gain reference (decimal)	Default gain reference (hex)
Pike F-032B, F-032C	200	C8h
Pike F-100B, F-100C	210	D2h
Pike F-145B, F-145C (15fps)	30 (15*)	1Eh (0Fh*)
Pike F-145B, F-145C (30fps)	85 (15*)	55h (0Fh*)
Pike F-210B	215	D7h
Pike F-421B, F-421C	200	C8h
Pike F-505B, F-505C	205 (130*)	CDh (82h*)
Pike F-1100B, F-1100C	228	E4h
Pike F-1600B, F-1600C	193	C1h

Table 202: Default gain references of Pike models

*: Firmware package version 00.03.00.01 or earlier

Firmware update

Firmware updates can be carried out via FireWire cable without opening the camera.

Note

For further information:

- Read the application note:
  How to update Guppy, Pike, or Stingray firmware
  at Allied Vision website or
- Contact your local Allied Vision distribution partner.

www

For our Sales locations see: https://www.alliedvision.com

Extended version number (FPGA/microcontroller)

The new extended version number (Pike firmware 3.× and later) for microcontroller and FPGA firmware has the following format (4 parts separated by periods; each part consists of two digits):

Special.Major.Minor.Bugfix

or

xx.xx.xx.xx

Digit	Description
1st part: Special	Omitted if zero Indicates customer specific versions (OEM variants). Each customer has its own number.
2nd part: Major	Indicates big changes Old: represented the number before the dot

Table 203: New version number (microcontroller and FPGA)

Digit	Description
3rd part: Minor	Indicates small changes Old: represented the number after the dot
4th part: Bugfix	Indicates bug fixing only (no changes of a feature) or build number

Table 203: New version number (microcontroller and FPGA) (continued)

Appendix

Sensor position accuracy

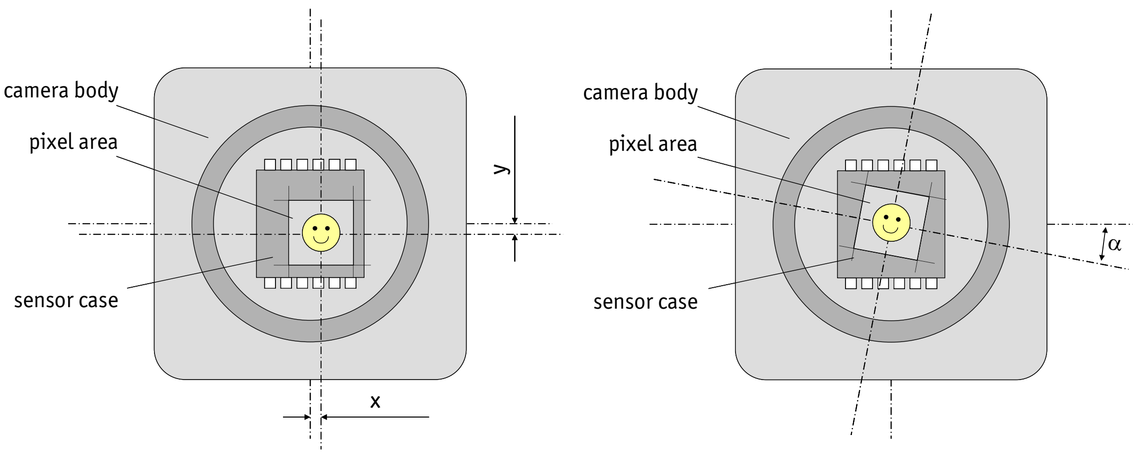


Figure 118: Sensor position accuracy

Criteria	Subject	Properties
Method of positioning		Optical alignment of the photo sensitive sensor area into the camera front module (lens mount front flange)
Reference points	Sensor	Center of the pixel area (photo sensitive cells)
	Camera	Center of the lens mount
Accuracy	x/y	+/- 0.1 mm (sensor shift)
	z	+0/-50 µm (optical back focal length)
	α	+/-0.5° (center rotation as the deviation from the parallel to the camera bottom)

Table 204: Sensor position accuracy criteria

Note

x/y tolerances between C-Mount hole and pixel area may be higher.

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